Low-Cost Testing of High-Precision Analog-to-Digital Converters

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Se Hun Kook

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Low-Cost Testing of High-Precision Analog-to-Digital Converters

Approved by:

Dr. Abhijit Chatterjee, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. David V. Anderson
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Linda S. Milor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Albert B. Frazier
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Suresh K. Sitaraman
School of Mechanical Engineering
Georgia Institute of Technology

Date Approved: June, 24th, 2011

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LIST OF SYMBOLS AND ABBREVIATIONS

SOC ---------- System On Chip

SOP ---------- System On Package

PCB ---------- Printed Circuit Board

DC ---------- Direct Current

AC ---------- Alternating Current

INL ---------- Integral Non Linearity

DNL ---------- Differential Non Linearity

SNR ---------- Signal to Noise Ratio

SNDR ---------- Signal to Noise and Distortion Ratio

ENOB ---------- Effective Number of Bit

THD ---------- Total Harmonic Distortion

LSB ---------- Least Significant Bit

FFT ---------- Fast Fourier Transform

ATE ---------- Automated Test Equipment

DUT ---------- Device Under Test

RMS ---------- Root Mean Square

TTM ---------- Time To Market

LPF ---------- Low Pass Filter

HPF ---------- High Pass Filter

FIR ---------- Finite Impulse Response

DFT ---------- Design For Test

BIST ---------- Built In Self Test

MARS ---------- Multivariate Adaptive Regression Splines

OSR ---------- Over Sampling Ratio

PSRR ---------- Power Supply Rejection Ratio

SR ---------- Slew Rate

GBW ---------- Gain Band Width

DIP ---------- Dual In-line Package

OP AMP ---------- Operational Amplifier

PSD ---------- Power Spectrum Density

AWG ---------- Arbitrary Waveform Generator

SPS ---------- Sample Per Second

PCA ---------- Principle Component Analysis

DMM ---------- Digital Multi Meter

SUMMARY

The advent of deep submicron technology has resulted in a new generation of highly integrated mixed-signal system-on-chips (SoCs) and system-on-packages (SoPs). As a result, the cost of electrical products has sharply declined, and their performance has greatly improved. However, a testing throughput still remains one of the major contribution factors to final cost of the electrical products. In addition, highly precise and robust test methods and equipment are needed to promise non-defective products to customers. Hence, the testing is a critical part of the manufacturing process in the semiconductor industry. Testing such highly integrated systems and devices requires high-performance and high-cost equipment.

Analog-to-digital converters (A/D converters) are the largest volume mixed-signal circuits, and they play a key role in communication between the analog and digital domains in many mixed-signal systems. Due to the increasing complexity of the mixed-signal systems and the availability of the new generations of highly integrated systems, reliable and robust data conversion schemes are necessary for many mixed-signal designs. Many applications such as telecommunications, instrumentation, sensing, and data acquisition have demanded data converters that support ultra high-speed, wide-bandwidths, and high-precision with excellent dynamic performance and low-noise. However, as resolutions and speeds in the A/D converters increase, testing becomes much harder and more expensive.

In this research work, low-cost test strategies to reduce overall test cost for high-precision A/D converters are developed. The testing of data converters can be classified as

dynamic (or alternating current (AC)) performance test and static (or direct current (DC)) performance test [1]. In the dynamic specification test, a low-cost test stimulus is generated using an optimization algorithm to stimulate high-precision sigma-delta A/D converters under test. Dynamic specifications are accurately predicted in two different ways using concepts of an alternate-based test and a signature-based test. For this test purpose, the output pulse stream of a sigma-delta modulator is made observable and useful. This technique does not require spectrally pure input signals, so the test cost can be reduced compared to a conventional test method. In addition, two low-cost test strategies for static specification testing of high-resolution A/D converters are developed using a polynomial-fitting method. The cost of testing can be significantly reduced as a result of the measurement of fewer samples than a conventional histogram test. While one test strategy needs no expensive high-precision stimulus generator, which can reduce the test cost, the other test strategy finds the optimal set of test-measurement points for the maximum fault coverage, which can use minimum-code measurement as a production test solution.

The theoretical concepts of the proposed test strategies are developed in software simulation and validated by hardware experiments using a commercially available A/D converter and designed converters on printed circuit board (PCB). This thesis provides low-cost test solutions for the high-resolution A/D converters.

CHAPTER Ⅰ

INTRODUCTION

Testing is one of the major factors in the semiconductor industry, which contributes to the total cost of electronic systems and devices and helps achieve the future success of the products. Among highly integrated circuits and systems, an analog-to-digital (A/D) converter is one of essential blocks in most mixed-signals and radio-frequency (RF) systems and determines the performance and quality of such systems. With increasing resolutions of the A/D converters, traditional test solutions become infeasible, and the cost of testing significantly increases because of expensive test equipment and exhausting measurement procedure of digital codes. Hence, the research works in this thesis focus on reduction in the test cost and measurement for the high-precision A/D converters compared to the traditional test methods. The Chapter 1 introduces standard test methodologies for the A/D converters and various research works from the past. Then, the research motivation and the contributions of the research work are discussed.

1.1. STANDARD A/D CONVERTERS TEST

Testing of data converters falls into two categories as follows [1]: (1) static (or direct current (DC)) performance test and (2) dynamic (or alternating current (AC)) performance test. The Static performance specifications include differential non-linearity (DNL),

integral non-linearity (INL), offset, and gain errors. Dynamic performance specifications include signal-to-noise ratio (SNR), total-harmonic-distortion (THD), signal-to-noise and distribution (SiNAD), and spurious-free dynamic range [2]. A low-frequency or DC test stimulus is used to measure the static specifications, while a high-frequency test stimulus is used for the dynamic specification measurements. In next Section 1.1.1 and 1.1.2, the details of static specifications and dynamic specifications are briefly discussed, and their conventional test methodologies are presented.

1.1.1 Static Specifications Testing

The static specifications of the A/D converters are measured using a low-frequency or a DC test stimulus. The static specifications are important because these specifications represent how well the A/D converters can convert an analog input voltage (or current) to a digital code.

1.1.1.1 Static Specifications

To help understand the static specifications better, a transfer function of an ideal 3-bit A/D converter with eight output code levels is shown in Figure 1 as an example. Note that an N-bit resolution A/D converter contains 2^N digital output codes. A set of input analog voltage values that correspond to a single digital code of the A/D converter is defined as a "*code widt*h". The analog signal value at which a digital code transitions from one code to

the next code is defined as a "*code transition point*". One code width of the ideal A/D converters is called one least-significant-bit (LSB), which is a ratio of the full-scale input value of the converters to the total number of digital codes, and this means that the code transitions are one LSB apart in the ideal case. For the ideal A/D converter transfer function, all code transition points fall along a straight line, and all digital codes have equal code width of 1LSB. For example, all code widths in Figure 1 are $1/8^{th}$ of the A/D converter full-scale voltage reference. However in reality, all code widths are not equal due to manufacturing imperfections, and this fact leads to a non-linear transfer function that cannot be depicted by the straight line shown in Figure 1.

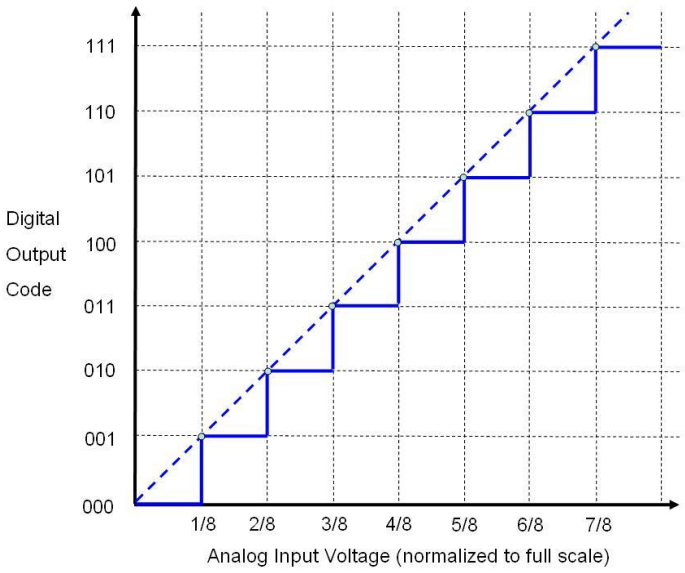

Figure 1. Transfer function of an ideal analog-to-digital converter.

The differential non-linearity (DNL) of a code is the difference between the actual code width and the ideal code width. Any deviation from one LSB is defined as the DNL error,

and its value can be positive or negative. The DNL for the A/D converters is described in Figure 2.

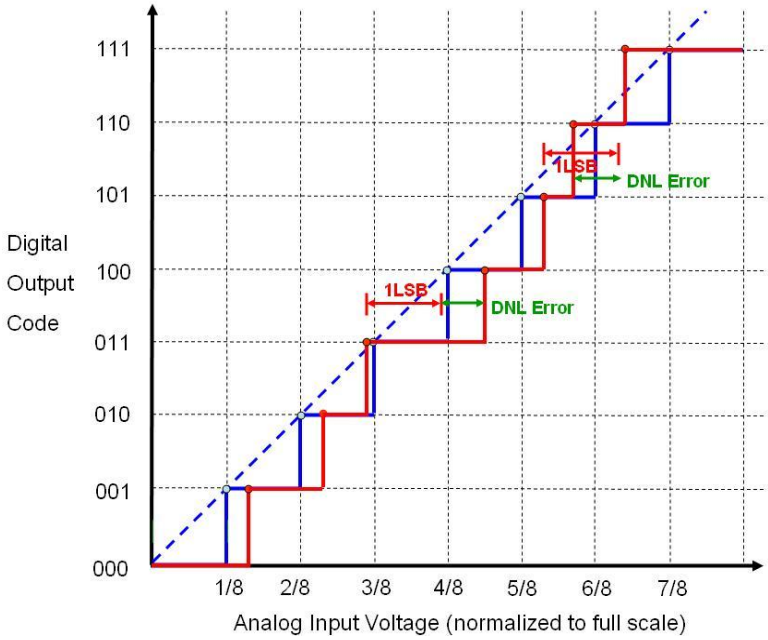

Figure 2. DNL in an A/D converter

Figure 3 shows the integral non-linearity (INL). The INL of a code is the deviation of the actual transfer function of A/D converters from its ideal transfer function as shown in Figure 3. This error is called integral non-linearity because it is an integral of the DNL. Most A/D converter datasheets present the INL plots for all digital codes, but a few datasheets note only a maximum INL error value.

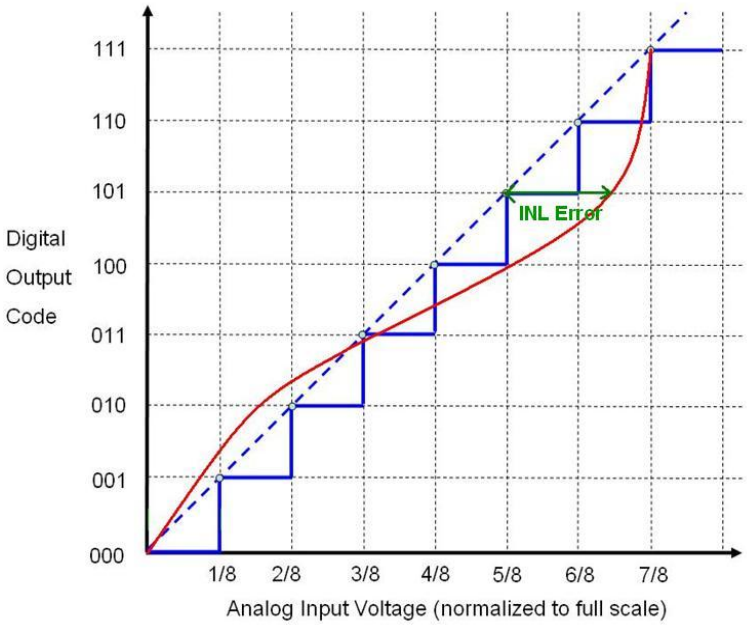

Figure 3. INL in an A/D converter

The gain error of the A/D converters is shown in Figure 4. This gain error is the deviation from the ideal full-scale value after the A/D converter is calibrated for an offset error. The gain error of the A/D converter indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. In general, this gain error and the offset error are simply calibrated out, and therefore, they are not as important as the DNL and INL errors.

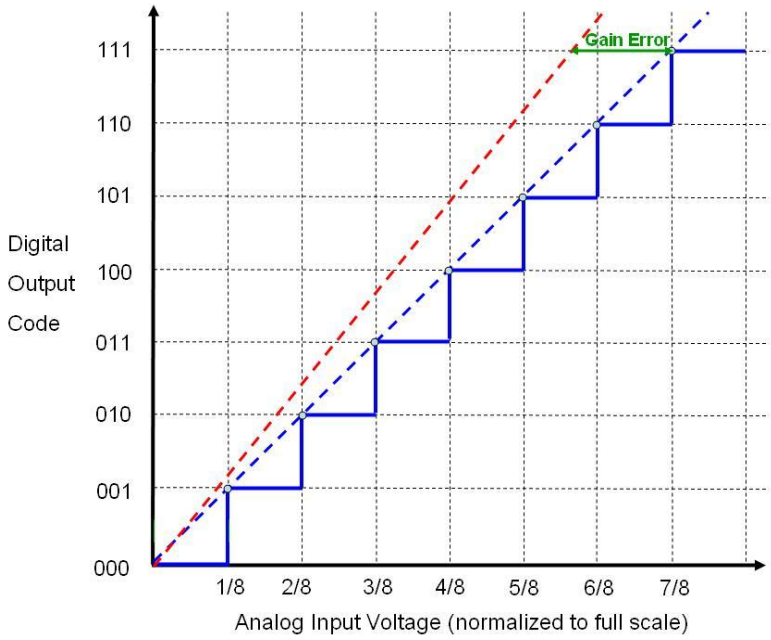

Figure 4. Gain error in an A/D converter

Figure 5 depicts the offset error, which is the deviation of the actual first-code transition from the ideal first-code transition. In many cases, -½ LSB of offset error is intentionally added by design to make the magnitude of quantization error less than ½ LSB because the quantization error can be shifted from 0 to 1 LSB to -½ LSB to +½ LSB. The quantization error is the difference between the actual analog value and quantized digital value as shown in Figure 6. This error is inevitable since analog signals are assumed to be continuous with infinite number of values, while digital values are a finite set of values that is determined by the resolution of the converters. The static specifications are usually expressed in LSB or as a percent of full-scale range (% error). All the static specifications can be determined once all code transition levels are measured.

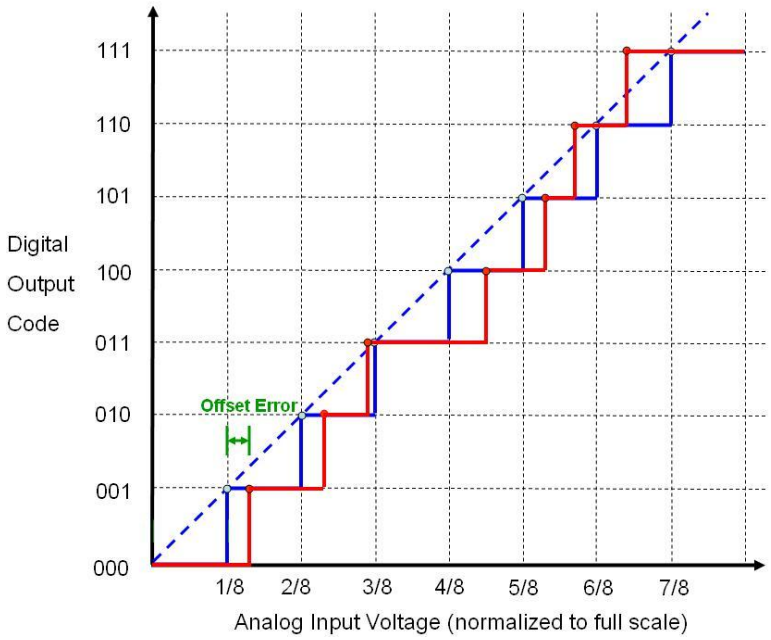

Figure 5. Offset error in an A/D converter

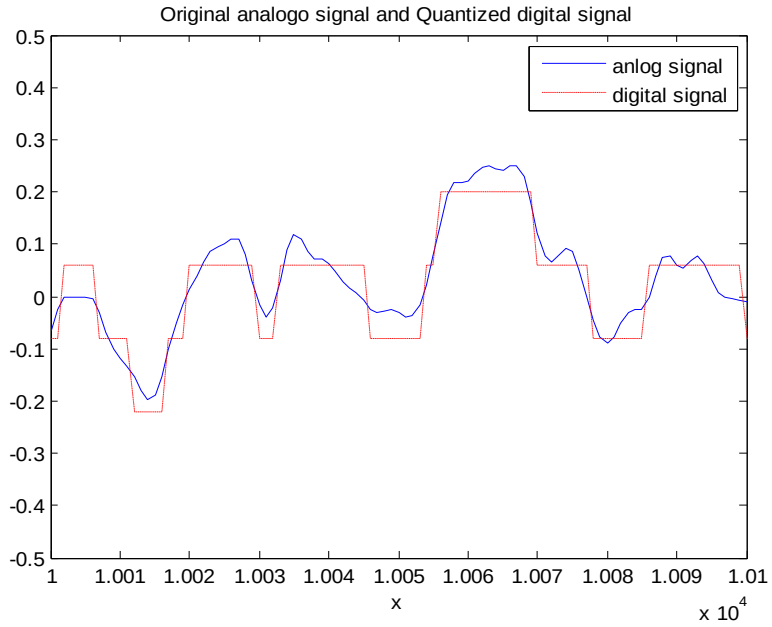

Figure 6. Original analog signal and quantized digital signal.

1.1.1.2 Current State of Art for A/D Converters Static Testing

The most standard test methodology for characterizing the linearity of the A/D converter is the histogram-based method, and Figure 7 describes the histogram-based test. In the histogram test method, a slow and precise periodic ramp signal or sinusoidal signal is applied to the A/D converters across a large number of cycles. The number of hits for each code of the A/D converter in response to the applied signal is then counted, and a histogram is plotted. This histogram is used to obtain a "*code edge transfer function"* of the A/D converter, which determines the individual code widths of each device. A basic concept of the histogram method using a ramp and a sinusoidal is almost similar with minor differences. In the histogram method using the linear ramp signal, a falling or rising ramp signal is applied to the A/D converter, and output code samples are captured at a constant sampling rate. This ramp signal must fall or rise through the entire conversion range of the A/D converter extremely slowly to make sure each digital code is *hit* several times. The number of hits per each code is collected and is proportional to the code width. The histogram plot for the number of code hits against output digital code is generated. For ideal and perfect A/D converters, the histogram must have a flat or an even distribution because each code must be hit the same number of times ideally. However, the histogram of a real A/D converter has an uneven distribution as a result of non-linearity of the data converter. Then, *LSB normalization* is performed by dividing the histogram distribution by the average number of hits for each code. This normalization procedure is shown in Figure 8. Note that the lowest and highest digital codes of the A/D converter have no defined code width, so the number of hits for these two codes is meaningless and is not counted. This LSB normalization histogram represents code

widths in LSB. First transition point from digital code 0 to digital code 1 must be found, and a binary search using a high-precision signal generator and measurement equipment is the most common method. Once the first transition point is found, and the code widths in LSB are converted into voltages or currents, the histogram plot can be converted to the code edge transfer function. The histogram method based on a sinusoidal signal follows the same steps. However, unlike the ramp-signal-based histogram that has the flat-distribution histogram, the histogram distribution would have a bathtub shape when using the sinusoidal signal because the sinusoidal signal has more inputs at lower and upper peaks than the input values at center. Due to this aspect, the LSB normalization from the number of hits is more complicated. In this case, LSB normalization can be performed using Mahoney's equation [2]. Then, the rest follows the same.

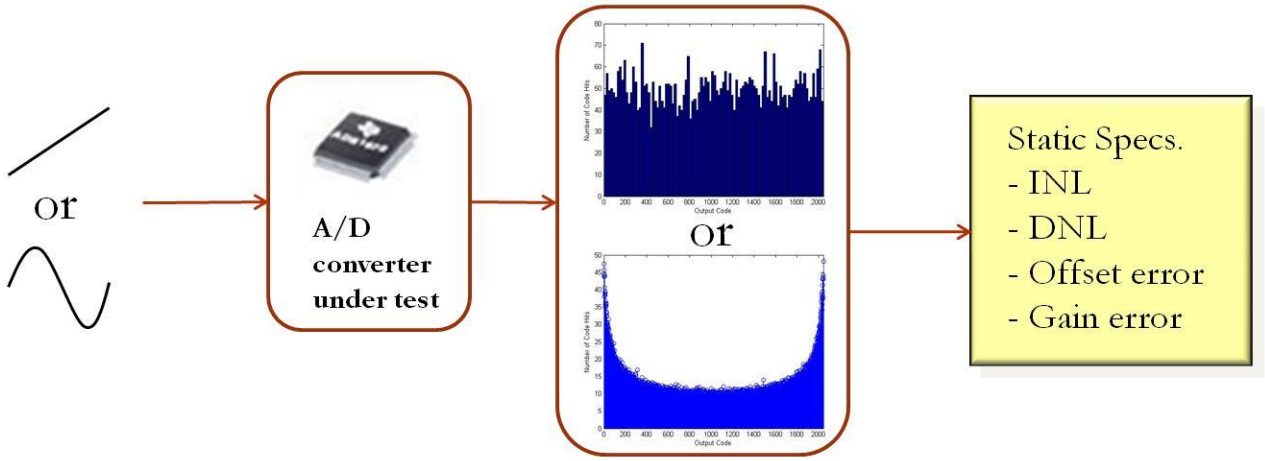

Figure 7. Histogram-based Test

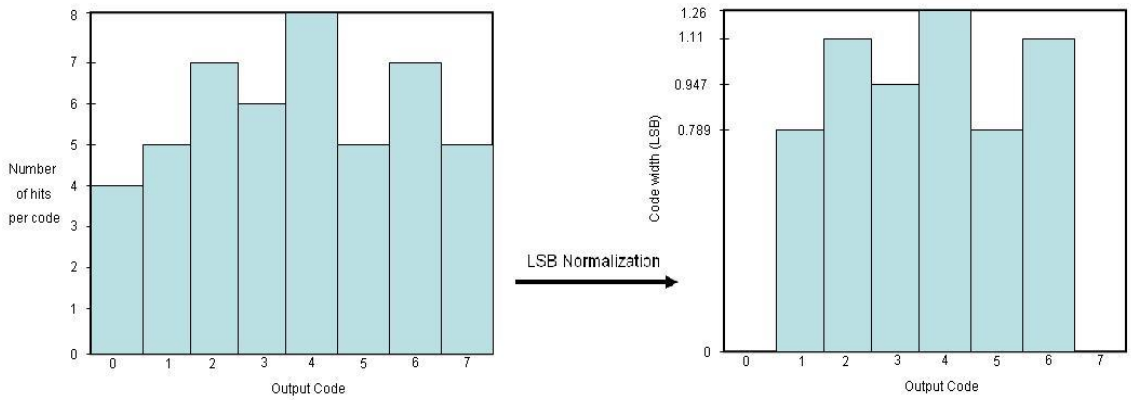

Figure 8. LSB normalization in histogram testing.

1.1.2 Dynamic Specifications Testing

The dynamic specifications of A/D converters are measured using a high-frequency test stimulus. These dynamic specifications are signal-to-noise ratio (SNR), signal-to-noise and distortion ratio (SINAD), effective number of bits (ENOB), total harmonic distortion (THD), and spurious-free dynamic range (SFDR). Meeting the requirements for the static specifications does not mean that the A/D converters perform well when the AC signals are applied. The dynamic specifications represent how well the AC input signal can be processed in the A/D converters against the noise and distortions.

1.1.2.1 Dynamic Specifications

While the static specifications described in Section 1.1.1 are important since they determine the DC accuracy of the A/D converter, dynamic specifications are also important for AC accuracy of the A/D converter. Especially for high-speed applications, these dynamic specifications are much more crucial than DC accuracy or static specifications because such dynamic specifications reveal the performance of the A/D converters in frequency domain. When the signal is processed in the systems, which are non-ideal and non-linear, additional contents are added, and the original input signal is degraded. Such additional contents can be the noises and distortions at the harmonics of the signal. Hence, the measurement of dynamic specifications exposes the performance of the signal processing in the presents of inevitable noise and distortion of the internal A/D converters.

Dynamic specifications can be measured from a spectral response of the A/D converters output. An example of the spectral response corresponding to a single-tone sinusoidal input signal with an input frequency of 2kHz is given in Figure 9. Once the noise floor, harmonic distortions, and signal power are measured from the spectral response of the A/D converters output, the dynamic specifications can be simply defined. Dynamic specifications are signal-to-noise ratio (SNR), signal-to-noise and distortion ratio (SiNAD), effective number of bits (ENOB), total harmonic distortion (THD), and spurious-free dynamic range (SFDR). SNR is a measure of a ratio of signal power to the noise, while SiNAD and ENOB show a signal power to the noise and distortion power. THD is a measurement of the extent of distortions, and SFDR shows the strength ratio of the signal to the strongest unwanted-spurious signal.

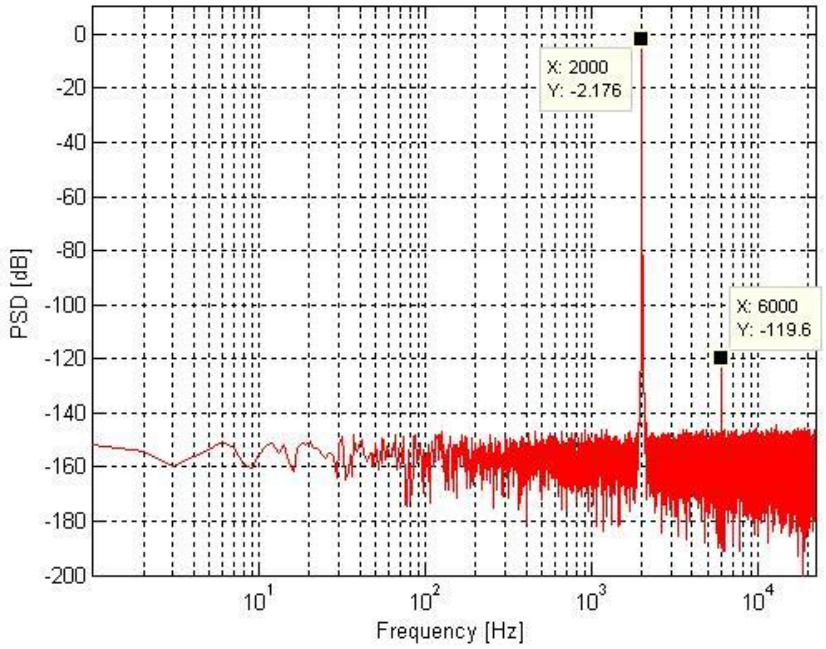

Figure 9. Power spectrum density (PSD) of the A/D converter output.

1.1.2.2 Current State of Art for A/D Converter Dynamic Testing

The most common test method to measure the dynamic specifications of A/D converters is fast-fourier-transform (FFT), and Figure 10 describes the conventional dynamic testing. Although various input signal sources such as a ramp or a triangular signal can be used, the most common source to measure the dynamic specifications is a single-tone sinusoidal signal due to its ease of analysis and generation at a low-cost. Thus, all the discussions here will be explained based on the assumption of using the sine-wave signal source.

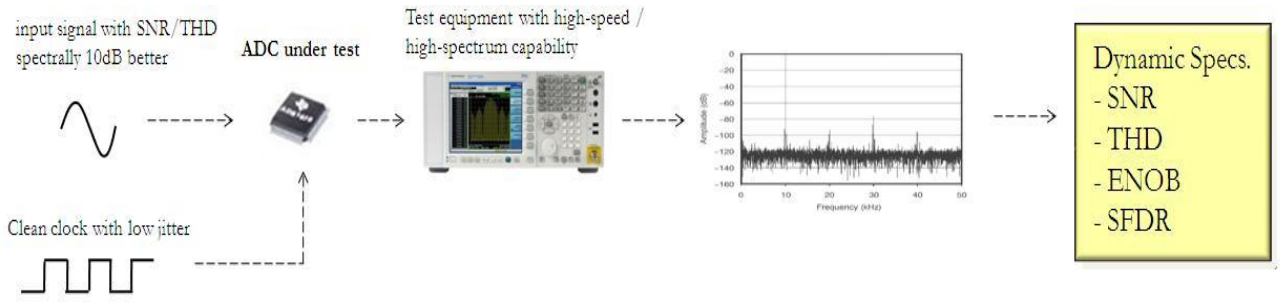

Figure 10. Conventional dynamic testing

The dynamic specifications test is performed by analyzing the behavior of the device under test (DUT) in frequency domain as shown in Figure 9 and Figure 10, and hence fast-fourier-transform (FFT) is mostly performed. The FFT transforms the same number of sampled outputs in time domain to frequency domain. The waveform is assumed to be continuous from $-\infty$ to $+\infty$ in FFT, but a finite set of samples are collected in the A/D converter test. To achieve the best results, a coherent sampling condition in Equation 1 is required when using the finite FFT. Without this coherent sampling condition, it is hard to prevent the power leakage in frequency bins. By satisfying the condition, the signal power in the FFT is assured to be contained within one FFT bin. Otherwise, an appropriate and dedicated windowing method is required.

$$\frac{M}{N} = \frac{f_T}{f_S} \qquad \text{Equation 1}$$

In Equation 1, M is the integer number of cycles, N is the total number of samples collected, f_T is the frequency of test input (or analog sine-wave input), and f_S is the sampling frequency of the device under test. For the best results, following conditions must be met:

1. M must be an integer number to make all the samples continuous.

2. N must be a power of 2 for the best use of efficient FFT.
3. The ratio of M over N must be irreducible because the same results can be achieved with fewer samples when the ratio is reducible.

Once the spectral response of the A/D converter is obtained using the FFT method with the coherent sampling condition, all the dynamic specifications can be easily defined.

Signal-to-noise (SNR) is one of the main dynamic specifications. SNR is a measure of a signal power relative to noise power and can be described as the ratio of a root means square (RMS) full-scale analog input to its RMS quantization error. For an ideal A/D converter, SNR driven by a pure sine-wave input ($s(t) = A\sin(2\pi t)$) with a period T and peak-to-peak voltage of 2A can be formulated as follows:

$$\text{Signal power} = \frac{1}{2\pi}\int_0^{2\pi} A^2 \sin(2\pi t)^2 \, dt = \frac{A^2}{2} \qquad \text{Equation 2}$$

$$\text{Quantization noise power} = \int_{-\Delta/2}^{\Delta/2} e^2 p(e) = \frac{\Delta^2}{12} \qquad \text{Equation 3}$$

$$\text{SNR}_{\text{ideal}}\ (\text{dB}) = \frac{SignalPower}{NoisePower} = 10\log_{10}\left(\frac{A^2/2}{\Delta^2/12}\right) = 6.02n + 1.76 \qquad \text{Equation 4}$$

, where e is the noise, n is the number of bits, and Δ is LSB of A/D converter, which is $\frac{2A}{2^n}$.

However, other noises in addition to quantization noise exist in the internal A/D converters. Thus, the actual SNR for a sinusoidal input signal is diminished by the other noise sources depending upon the level of total noises. Its theoretical formulation is given as

$$\text{SNR (dB)} = \frac{Signal\_Power}{Total\_Noise\_Power} = 6.02n + 1.76 + 10\log_{10}\left(f_S / 2f_{\max}\right) \qquad \text{Equation 5}$$

, where f_S is the sampling rate of A/D converter, and $f_{\max}$ is the maximum bandwidth of the input tone.

Signal-to-noise and distortion ratio (SiNAD) is similar to SNR. The difference is that SiNAD includes distortions as noise. Hence, SiNAD is the ratio of RMS signal power to the power of noise and distortion. In general, 2nd to 5th order harmonic distortions are significant and taken into account. Equation 6 provides SiNAD.

$$\text{SiNAD (dB)} = 20\log_{10}\left(A_{signal}(rms) \Big/ A_{noise+distortion}(rms\right) \quad \text{Equation 6}$$

, where $A_{signal}(rms)$ depicts the RMS output signal level, and $A_{noise\_distortion}(rms)$ is the RMS sum of all spectral components below the Nyquist frequency, excluding DC. Both SNR and SiNAD depend on the amplitude and frequency of the input tone.

Effective number of bit (ENOB) is a measure of a real resolution compared to its ideal resolution of the converters. Equation 7 describes ENOB in mathematical formulation.

$$\text{ENOB (bit)} = N\log_2\left(A_{measured\_error}(rms) \Big/ A_{ideal\_error}(rms)\right) \quad \text{Equation 7}$$

, where $A_{measured\_error}(rms)$ is the averaged error and $A_{ideal\_error}(rms)$ is the quantization error. This also can be re-written in terms of SiNAD as

$$\text{ENOB} = \frac{(SiNAD - 1.76)}{6.02} \quad \text{Equation 8}$$

Total harmonic distortion (THD) is a measurement of powers in all the harmonic distortion. It is the ratio of the sum of all the powers of harmonic components to the power of the fundamental frequency. Thus, a lower THD represents better performance of A/D

converters. The harmonic distortion components are found at integer multiples of the input tone. All the harmonic distortion components contribute to THD, but first 5 to 10 harmonics are the most significant. THD can be calculated from the FFT normalized-magnitude graph, and its formulation is shown in Equation 9.

$$\text{THD (dBc)} = 20\log_{10}\left(\sqrt{\frac{\sum_{i=2}^{K} A_{harmonic(i)}}{A_{[f_{in}]rms}}}\right) \qquad \text{Equation 9}$$

, where $A_{harmonic(i)}$ is the RMS amplitude of i-th order harmonic, and $A_{[f_{in}]rms}$ is the RMS fundamental amplitude.

Spurious-free dynamic range (SFDR) is another important dynamic specification because the harmonic distortions and spurious signals are unwanted spurs in the output spectrum. SFDR indicates the dynamic range of an A/D converter describing the in-band harmonic characteristics of the A/D converter. SFDR is the ratio of RMS amplitude of the fundamental (the maximum signal component) to the RMS value of the largest distortion or spur component in a specified frequency range as shown in Equation 10.

$$\text{SFDR (dBc)} = 20\log_{10}\left(\frac{A_{[f_{in}]rms}}{A_{[spur\_\max]rms}}\right) \qquad \text{Equation 10}$$

, where $A_{[f_{in}]rms}$ is RMS amplitude at the fundamental frequency, and $A_{[spur\_\max]rms}$ is the RMS amplitude of the averaged DFT value of the largest-amplitude harmonic or spurious signal component over the entire Nyquist band.

1.2. PREVIOUS WORK

Testing of the A/D converters is an active and well-defined research topic, and various research works have been proposed in the past. For decades, digital-signal processing has replaced almost all analog-signal processing in modern integrated circuits and systems because the digital technique has great advantages over the analog technique such as less power consumption, noise immunity, small size, and easy design. As a result, a number of analog and digital circuitries have been integrated together in one system. These highly integrated systems are inevitably dependent on the performance of the data converters due to the fact that data converters provide the interface between analog and digital circuitries in such highly integrated systems. Therefore, the performance quality of the data converts has become extremely important. Consequently, the importance of testing data converters obtains so much attention from the industry and research community that testing of the data converters becomes a hot research topic. Research approaches in A/D converters testing can include an input stimuli generation, modeling techniques, diagnosis, statistical approach, design-for-test (DfT), built-in-self-test (BIST), and et cetera.

First, the institute of electrical and electronics engineers (IEEE) gives a standard for testing the A/D converters in [3]. This standard guides terminologies and definitions in the A/D converter testing and test methodologies with error sources of the A/D converters. The A/D converter testing using this guideline is provided in [4]. This reveals that a highly clean and pure signal source is needed for testing A/D converters. Therefore, the generation of high-precision and linear signal sources as test stimuli is proposed in [5]-[7], while A/D

converter test methodologies using non-linear and imprecise signal sources are also proposed in [8] – [18].

In addition, modeling for the A/D converter testing is also a well-defined research area. The authors in [19] and [20] propose a fault model for A/D converter testing. The authors review a general A/D converter modeling and testing in [21] and persist that modeling and testing must be related. Behavioral error modeling of A/D converters INL is described in [22]. Linear modeling for A/D converter testing is described in [23]-[27]. In A/D converter testing using the linear modeling, the linearity test time can be reduced by measuring only a defined subset of transition levels, which is much less than the total number of codes. Hence, the test cost can be significantly reduced [28] as compared to the conventional histogram test. Fault diagnosis for the A/D converters [29]-[33] and design for testability (DfT) [34]-[38] are also proposed. These fault diagnosis and design-for-testability techniques are carefully designed depending on the types of A/D converters. Since the internal accessibility to the A/D converter components in integrated system gets harder, these techniques become a good solution in some applications. Built-in-self-test (BIST) is another solution. BIST techniques use extra circuitries to test A/D converters in systems, and thus it requires an extra overhead area. However, BIST provides easier testability without any other expensive automatic test equipment (ATE) and tough access to the A/D converter pins. As a matter of fact, the small overhead silicon area and precise stimuli generator are major issues to be solved. The authors in [39] use an on-chip sigma-delta D/A converter to generate sinusoidal signal as its stimulus. The BIST based on oscillation frequencies is proposed in [40]. Polynomial-curve fitting for A/D converter BIST is introduced in [41]. A partial BIST method by monitoring the reduced

number of bits externally is proposed in [42]. Precision signal generators on BIST scheme are proposed in [7] and [43]. Techniques in [8]-[12] are also possible techniques for BIST. Many other BIST approaches are being proposed and researched now.

1.3. MOTIVATION

In Chapter 1.3, the motivation of the research work in this thesis is discussed. First, the test economy is briefly outlined with discussions of the importance of testing and the cost of testing. Then, the issues in A/D converters testing and problems associated with current state-of-arts for testing the A/D converters are summarized.

1.3.1 Test Economy

In the semiconductor industry, manufacturing cost has been significantly reduced over the decades, but testing techniques still stand behind fabrication and integration techniques. Further, as the integration technique has been advanced, the testing has become more challenging and expensive because (1) many sub-circuits and sub-systems are integrated together in a small chip or package, so the access to such sub-chips and sub-systems is extremely limited, and (2) testing such high-performance systems requires expensive automatic test equipments (ATEs), which cost multi-millions of dollars. Figure 11 shows Moores's law for test capital in left and Moore's law for test capital in comparison to the

chip fabrication cost in right. From this Figure 11, while the cost of the fabrication per a transistor is dramatically reduced for a few decades, the cost of the test for a transistor is increased.

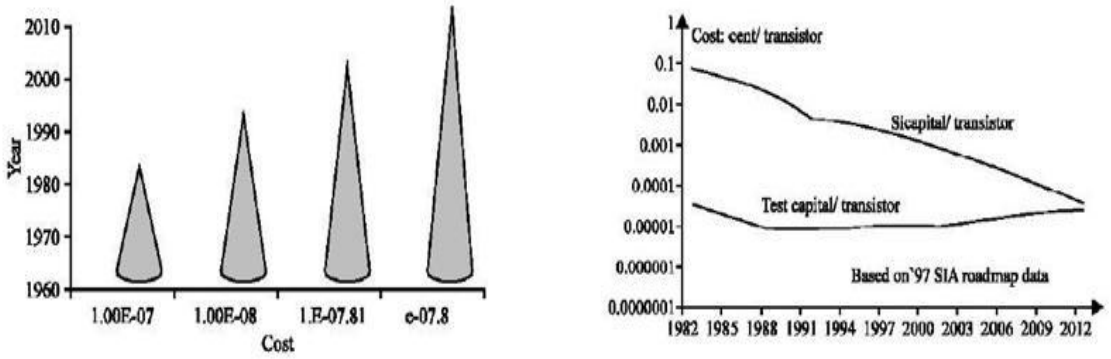

Figure 11. Moores's law for test capital [44].

Figure 12 presents the contribution for the manufacturing cost of electrical products. As seen in Figure 12, the cost of the testing takes a large portion of the final cost of electrical products besides fabrication and design costs, which is close to a half of the total cost. To manufacture competitive electrical products in the semiconductor industry, reduction in the test cost is one of the key factors. Without the cost reduction of the testing, the final cost of the products might be higher than other competitors, which cannot bring the success to the manufacturers. In addition, business must pursue high-margins, so all the manufacturers in the semiconductor industry are looking for low-cost production solutions.

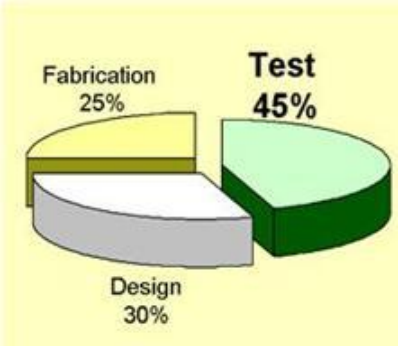

Figure 12. Manufacturing cost of electrical products [45].

Testing of the semiconductor devices must consider (1) time-to-market, (2) yield coverage, (3) fault coverage, and (4) testing capital. The time-to-market (TTM) is the length of time that takes to deliver the first product for sale. This time-to-market is important in the technology industry that develops and manufactures innovative products. Many believe that the shorter the product project, the less it will cost. Further, early time-to-market can allow higher initial selling prices with less competition than a lengthy time-to-market. The early time-to-market demonstrates its product innovation and technical strength of the business. To avoid the lengthy time-to-market, the time for all the design, fabrication, and testing must be reduced. The testing step, which is the last procedure before sale, may take a long time to promise the best quality and achieve the business success, and this long test time is non-ideal. Yield and fault coverage are also important and refer to the quality of the test. Yield coverage refers to rejection of quality or good devices, while the fault coverage refers to acceptance of defective or bad devices. Before delivering products to the customers, all the products must be tested and passed to ensure that the products meet the datasheets and qualifications. The devices that fail the test must be

discarded. Test solutions that achieve high-yield coverage and high-fault coverage can save the total product cost and guarantee the quality of the products. At last, the testing capital consists of tester capital, handler capital, test house and maintenance, and test development, which directly contributes to the total test cost. Figure 13 describes the test cost with the test time. Figure 13 shows that the overall testing cost extremely depend on the cost of test instrumentation and test time. It is true that less expensive test equipment does not always reduce the test cost as compared to using more expensive test equipment if a long test time is required. If more expensive instrument, $24 million tester in Figure 13, can significantly reduce the total test time than less expensive equipment, $100,000 tester in Figure 13, the use of more expensive equipment might reduce the overall test cost and eventually the final product cost. Hence, a reasonably fast test solution with low-cost test equipment would be an ideal solution.

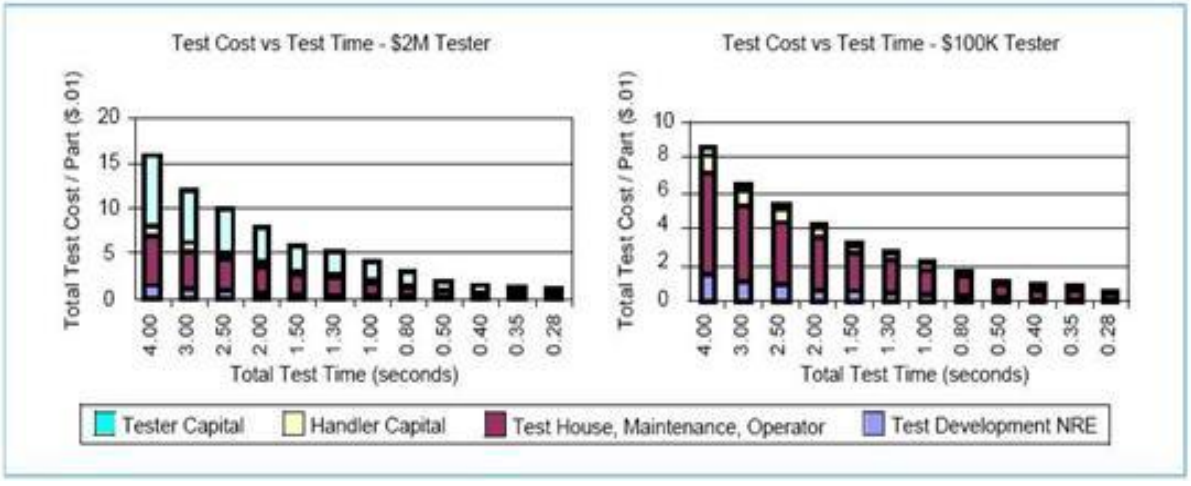

Figure 13. Test cost versus test time [46].

1.3.2 Issues Associated with A/D Converters Test

Analog-to-digital converters (A/D converters) convert analog voltages or currents to digital codes, and the number of digital codes depends on the resolution of A/D converters. Since a certain range of analog signal values represents a specific single digital code, a transfer function of A/D converters has a many-to-one mapping function. In this sense, as the resolution increases, the number of codes increases, and the digital codes must shift from one to next in a smaller analog signal value change than lower resolution data converters. Therefore, high-resolution A/D converters have the capability to detect extremely small changes in analog signal values and thus are desired for sensitive measurements. The linearity requirements of these data converters are usually stringent enough to ensure precise measurement. As a result, static performance testing of high-resolution A/D converters requires test instrumentation that has higher precision digital-to-analog conversion capability or sine-wave generators than the A/D converters under test. Such instruments are extremely expensive. Furthermore, a large number of samples need to be collected to guarantee the test quality, which leads to a large test time. Currently, 24-bit resolution A/D converters become common in the market and are used in various applications. A common 24-bit A/D converter includes more than 16 million codes in 5V full-scale range, and each digital code changes in much less than micro volts. Thus, linearity requirements for the high-resolution A/D converters lead to complex test solutions and significantly contribute toward increasing the overall manufacturing cost of these products. In addition, analog test capabilities such as test systems with low-noise floor and

synchronization and a high-frequency platform are required for dynamic specifications testing. A spectrally pure and high-frequency signal with at least a 10 dB better signal-to-noise ratio (SNR) and total-harmonic-distortion (THD) than the A/D converters under test is needed to stimulate the A/D converters. Furthermore, output measurement equipment must be capable of accurate measurements. The sampling clock must have low-jitter specifications when testing dynamic specifications. This equipment is also remarkably costly. Further, lengthy test procedures can affect the time-to-market process for these devices. Hence, test cost reduction is crucial to reduce the overall manufacturing cost of these devices and to ensure commercial success.

The A/D converters can be divided into two groups as follows: (1) high-precision A/D converters and (2) high-speed A/D converters. These two groups of A/D converters have different issues to solve. Currently, the A/D converters with a resolution of 4-bit to 24-bit and a sampling rate of 15 sample per second (SPS) to 3G SPS are commonly available in the market. Different architectures are built for specific resolution and sampling rate. General data conversion rates and resolutions for different structures of A/D converters are outlined as follows:

1. A flash A/D converter (also called direct-conversion A/D converter): This A/D converter has the fastest data conversion in general (10M SPS to over 1G SPS) but low-precision, which is 8-bit or fewer. This A/D converter type requires a large die size and is generally used for video, wideband communications, or optical applications.

2. A pipeline A/D converter (also called subranging quantizer): Similarly, this type is also relatively fast (over 1G SPS) and low-to-mid-resolution (8-bit to 14-bit) A/D converter. However, this A/D converter usually has higher resolution than the flash A/D converter and takes advantages of successive approximation A/D converters and flash A/D converters. It requires a small die size.
3. A successive approximation A/D converter: This A/D converter has more complicated structures than other types of A/D converters but has good resolutions (up to 18-bit) with low-to-mid data conversion (up to 1G SPS).
4. A sigma-delta A/D converter: Sigma-delta A/D converter uses a sigma-delta modulator which generates 1-bit output data stream. This A/D converter has high-resolution up to 24-bits and low-sampling rate (less than 5M SPS). The sigma-delta A/D converter is inherently linear. This A/D converter is used mainly in audio application.
5. A ramp-compare A/D converter (also called integrating A/D converter): This type of A/D converter is not generally popular. Resolution of this A/D converter is as good as sigma-delta A/D converter but has much less sampling rate (usually less than 1k SPS). The advantage of this A/D converter is a simple structure.
6. Incremental A/D converter: Incremental converter is based on the sigma-delta A/D converter architecture but has two main differences. The integrator and digital counter are reset at every new conversion, and conversion rate is 2^{n+1} clock period rather than oversampling ratio and hence is much slower than the sigma-delta A/D

converter. This A/D converter also has high-resolution (24-bit or higher) and is used in measurements and instrumentation applications.

For the high-precision A/D converter testing processes, an extremely large number of samples are needed to be collected due to a large number of digital codes. In addition, high-precision A/D converters have low-sampling rates in general. As a result, collecting a huge number of samples at low-speed sampling rates means a long test time. This long test time directly implies high test cost. As the resolution of A/D converters increases, the digital code levels, which must be tested, increase with a power of two. Measurements across all the digital code levels of data converters with 18-bit or higher resolution are not physically practical and are extremely exhausting. Further, the performance requirement for the generation of extremely high-resolution input signal is another big issue because the input signal source must be more linear than the data converter under test. In general, the resolution and linearity of input stimuli must be at least 3-bit higher than the resolution of A/D converters under test. High-resolution A/D converters must have the capability to detect significantly small changes in analog signals. This implies that the input signal also must have the capability to generate extremely small changes in analog signals to guarantee the test quality. For example, a common 24-bit A/D converter with an input voltage range of 0V to 5V would have one LSB of approximately $0.3\,\mu$V, which means that each digital output code of this A/D converter is varied by $0.3\,\mu$V. The input source must have a minimum resolution of a 27-bit linearity for testing the 24-bit A/D converter.

For the high-speed A/D converters, a high-frequency platform is required. An input source must generate high-frequency signals with reasonable purity, and measurement

equipments must be able to capture all the high-frequency components accurately. Recommended input signals must have THD and SNR about 10 dB better than the A/D converters under test. Extremely expensive test equipments are required for generating such pure input signals and capturing output signals. In addition, clock jitters must be taken into account when testing high-speed A/D converters in dynamic specifications test because clock jitters dominate all the other noise sources at high-frequency measurements. Sampling clocks with low-jitter are available, but such clocks are also extremely expensive. To reduce the spectral leakage in the dynamic test, a coherent sampling cannot be ignored. Use of the coherent sampling lets the fundamental component and each of its harmonics fall precisely on a single bin of the spectrum preventing any spectral leakage. Consequently, all the test equipments must support this coherent sampling. Otherwise, specific filters, windowing methods, or other methods must be additionally required.

For testing both static and dynamic specifications, a long test time and high-performance and expensive test-platforms are required. Consequently, the long test time and expensive test methodologies significantly increase both the production test cost and the final product cost.

1.4. CONTRIBUTION

A main goal of this thesis is to overcome the current issues of the A/D converters testing and develop low-cost test solutions for the high-precision A/D converters. Main contributions of the research work in this thesis are summarized below:

1. Alternate-based low-cost test strategy for dynamic specification testing of high-resolution sigma-delta A/D converters: Dynamic specifications are accurately predicted using a concept of the alternate test. For this test purpose, the output pulse stream of a sigma-delta modulator is made observable and used. This technique does not require spectrally pure input signals, so the test cost can be reduced as compared to the conventional FFT test, and the use of the alternate test can save the overall test time and simplify the test procedure by predicting all the specifications at one time.
2. Signature-based low-cost test strategy and diagnosis methodology for dynamic specification testing of high-resolution sigma-delta A/D converters: This signature-based test strategy adopts the test setup in the above alternate-based test method, which makes the use of sigma-delta modulator output. This methodology uses an optimized multi-tone test signal, possibly of lower resolution than A/D converter under test, which saves the overall test cost. In addition, the method allows diagnosing defective devices. The technique eliminates the use of a supervised learner with a training set of devices, which is required in the above alternate-based test.
3. A low-cost strategy for static specification testing of high-resolution A/D converters: This test strategy is based on a polynomial-fitting method. In this methodology, techniques called scaling and segmentation are used with the polynomial least-square-fitting method. In this test scheme, the test cost is reduced since no expensive high-precision stimulus generator is required, and fewer samples are measured compared to the conventional test method.

4. A low-cost optimal static specification testing of high-resolution A/D converters using restricted code measurements: This test methodology is also based on the polynomial-fitting method, which is similar to the above scaling and segmentation technique. However, the measurement is further reduced as compared to the scaling and segmentation technique. With the penalty of using high-precision signal generator, this technique defines the minimum necessary test code points. In addition, the method provides an optimization-based search technique that defines the test escapes and reveals the characteristics of such devices.

A summary of the proposed research works in this thesis with the contributions is illustrated in Figure 14.

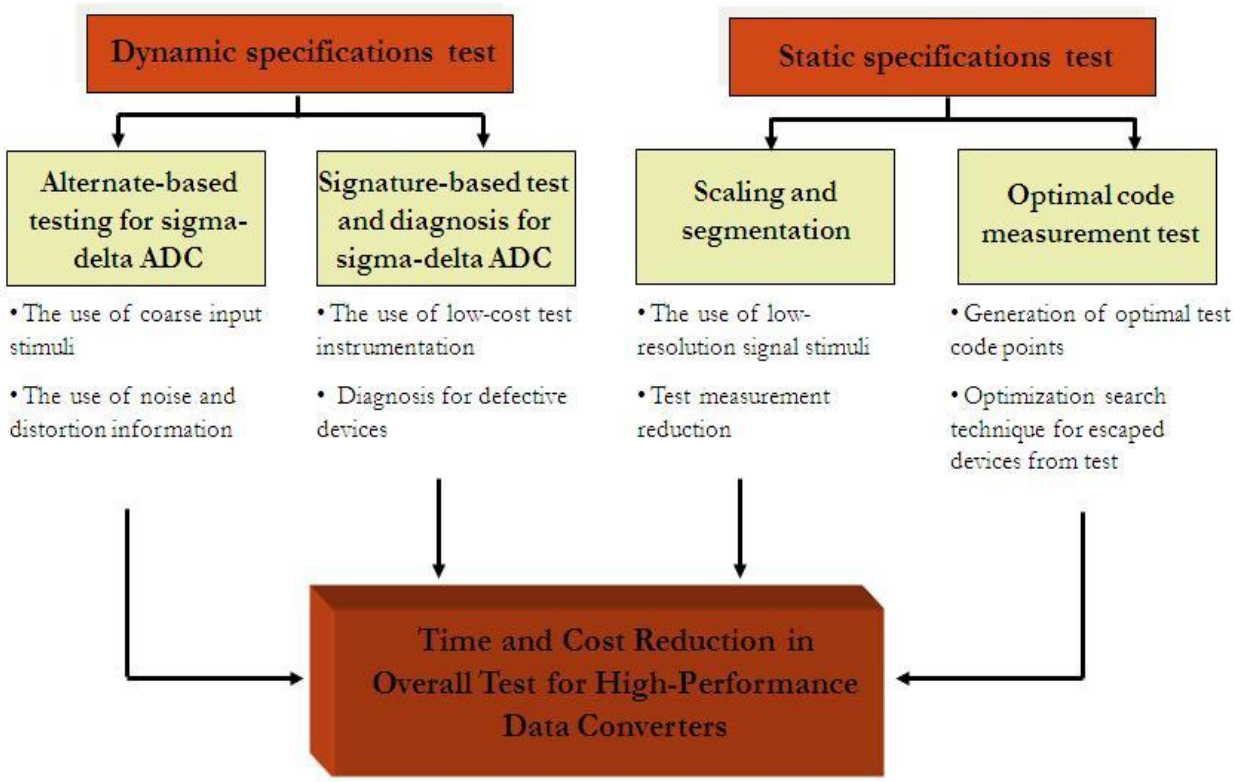

Figure 14. Efficient testing of high-resolution A/D converters.

CHAPTER Ⅱ

ALTERNATE-BASED DYNAMIC TESTING OF HIGH-RESOLUTION SIGMA-DELTA A/D CONVERTERS

In Chapter 2, a low-cost test methodology for the dynamic specifications of high-precision sigma-delta (ΔΣ) analog-to-digital converters (A/D converters) is presented. Dynamic testing of the data converters requires an input test stimulus with total harmonic distortion (THD) and signal-to-noise ratio (SNR) about 10dB better than the data converters under test. The cost of generating such spectrally pure signal is extremely expensive for the high-SNR sigma-delta A/D converters. The Chapter 2 will introduce the proposed test methodology for the high-precision sigma-delta converters using spectrally less pure and less linear signal sources than devices under test (DUTs). The use of such input signal can help ease the tight requirements for the test stimulus and lead to the cost reduction. The proposed test methodology is based on the alternate-testing technique proposed in [53]. The goals and objectives of the proposed methodology are summarized as follows:

1. The proposed methodology enables testing of the dynamic specifications (ENOB, THD, and SNR) of the high-precision sigma-delta A/D converters (16-bit to 24-bit) using low-cost test instrumentations, possibly lower resolution than the DUT itself.
2. Through the choice of appropriate test stimulus design, test access point selection and test response analysis techniques, the proposed methodology significantly

amplifies the sensitivity of the test measurement to the converter non-idealities, thereby enabling significant reduction in the test time.

The rest of the Chapter 2 is organized as follows: Section 2.1 discusses a brief description of the issues for the dynamic test of the high-precision data converters and prior works proposed by other researchers. Detail of the proposed low-cost test approach is provided in Section 2.2. Then, Section 2.3 presents the implementation of the proposed method and sensitivity analysis, which are the key benefits of the proposed approach. Finally, the validations of the proposed methodology are presented using simulation results in Section 2.4 and hardware experiment in Section 2.5.

2.1. PREVIOUS WORK

This Chapter 2.1 discusses the issues associated with the dynamic testing for the high-precision data converters, and a summary of various research works involving the dynamic testing of the A/D converters is presented.

The sigma-delta A/D converters are inherently high-resolution converters with excellent THD and SNR due to their inherent over-sampling, averaging, and noise shaping properties. For this reason, the generation of the test input stimulus with at least 3-bit higher resolution and linearity and spectrally 10dB better in SNR and THD than the A/D converters under test is extremely challenging and costly.

Several methods for the dynamic test of the sigma-delta A/D converters have been proposed in past years. The use of digital stimulus for testing the sigma-delta converters is

presented in [39], [47]-[49]. Digital stimulus is generated by software in [47]-[48]. The above test methods require the use of op-chip digital stimulus generation resources and the analysis of large bit-streams of data. In [50], an on-chip generation of band-limited test stimulus is investigated, but the method requires the use of special analog filters. The authors in [51] propose to use pseudo-random sequences to test a sigma-delta modulator with the objective of characterizing the same. In [52], the author proposes the use of a quantizer node as a new test node in the sigma-delta modulator and uses the noise transfer function of the modulator to measure its gain, SNR, and THD specifications. This methodology requires the use of a high-fidelity input signal that can be used to characterize loop filters with minimum error. In [14], a technique called SRE (Spectrally Related Excitation) that uses two imprecise input stimuli to measure dynamic specifications is proposed. The spectral relationship between two input signals, one applied directly to the converter and the other a filtered version of the first, is used to differentiate between the linearity of the test input signal and that of the DUT. Then, this is used to generate accurate values for specifications of the DUT such as SFDR than possible using only a single test.

Current test solutions for the high-precision A/D converters as described above require additional resources to generate test input stimuli and do not address the issue of converter test-time reduction in a significant manner. In the next Section 2.2, the proposed test methodology for the dynamic specifications of high-precision sigma-delta A/D converters that relaxes the tight requirement for the input stimulus and reduces the overall test time will be described.

2.2. PROPOSED METHODOLOGY

The detail of the proposed methodology is presented in Chapter 2.2. The proposed methodology is to test the dynamic specifications of the high-resolution sigma-delta A/D converters. In the proposed approach, the back-end digital and decimation filters of the sigma-delta A/D converters are turned off, and the digital pulse sequence at the output of the sigma-delta modulator is made externally observable for a test purpose. It is seen that ENOB, THD, and SNR of the converter can be determined with significantly increased sensitivity to device non-linearity and noise allowing the use of less than an ideal input stimulus and significantly reduced test time. The back-end filters are then tested using traditional digital test techniques. Following sections will provide detailed description of the proposed methodology. First, the overview of the sigma-delta A/D converters is discussed in Chapter 2.2.1. Then, the approach of the proposed methodology is provided in 2.2.2.

2.2.1 Overview of Sigma-Delta A/D Converters

The sigma-delta A/D converters, also called over-sampling converters, consist of a sigma-delta modulator, digital filters, and digital decimators. Figure 15 shows the architecture of the sigma-delta A/D converter. As seen in Figure 15, the sigma-delta modulator samples the input analog signal at a relatively high-sampling rate (over-sampling rate), far exceeding Nyquist sampling rate, and generates a serial 1-bit data stream, where

the number of pulses represents the average value of the analog input signal. The overall transfer function of the sigma-delta A/D converter consists of the signal transfer function and noise transfer function. The signal transfer function operates as a low-pass-filter (LPF), while the noise transfer function works as a high-pass-filter (HPF). The FFT of the oversampled bit-stream at the output of the sigma-delta modulator contains high-frequency noise as a result of the noise-shaping property of the sigma-delta converter that "pushes" the noise power from the bandwidth of the signal (in-band components) to the higher frequency components of the oversampled output of the sigma-delta converter (out-of-band components).

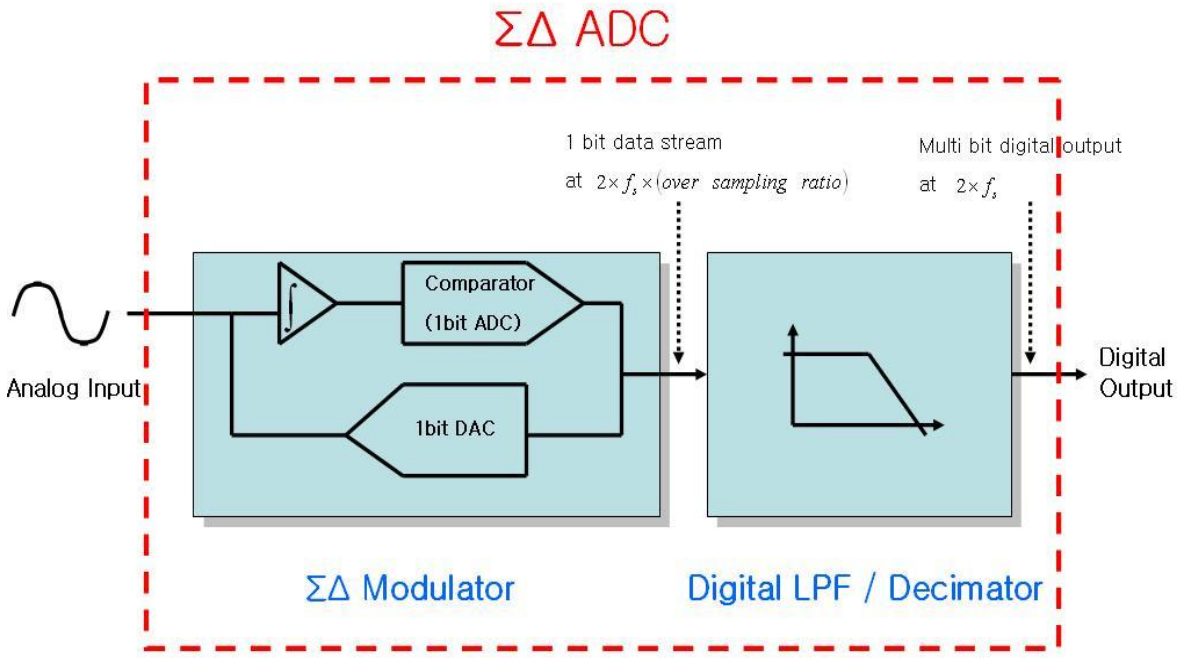

Figure 15. Structure of sigma-delta A/D converter

The power spectrum density plot of the sigma-delta modulator and noise shaping are shown in Figure 16. Noise in this high-frequency band is removed by an appropriate digital filter, and a digital decimator is used to generate a multi-bit digital output at the Nyquist rate as shown in Figure 15. The output of the sigma-delta A/D converter contains only in-band component with low-noise floor. In this manner, the noise level in the band of interest is reduced. This allows the sigma-delta A/D converters to achieve high-resolutions with high-SNRs.

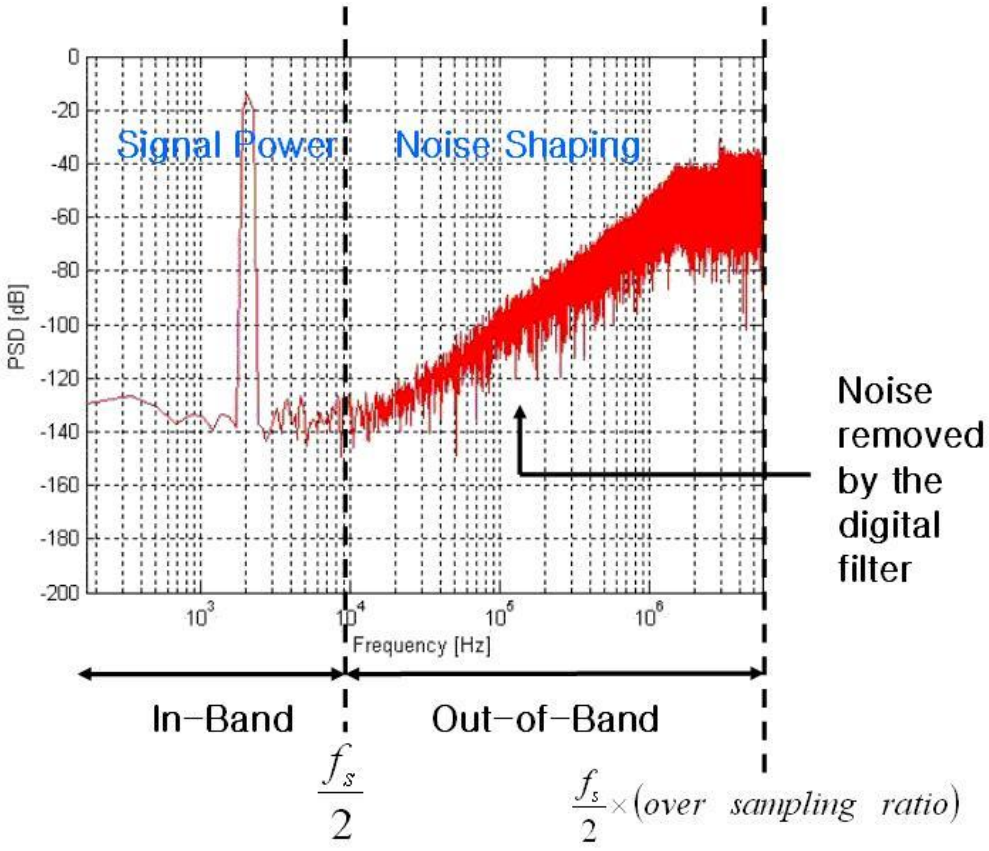

Figure 16. Effect of digital filter on noise shaping

In general, not only 1-bit sub-A/D converters and 1-bit sub-D/A converters but also multi-bit sub-A/D converters and sub-D/A converters can be used depending on the applications and requirements. The sigma-delta modulator of Figure 15 is a first-order modulator, and higher order modulators contain larger numbers of feedback loops and thereby larger numbers of poles in the sigma-delta transfer function. The number of the feedback loops indicates the order of the sigma-delta modulator. Higher order sigma-delta A/D converters allow more noise to be pushed to out-of-band high- frequency components than lower order sigma-delta A/D converters. Higher SNR and resolution can be accordingly achieved than lower order sigma-delta A/D converters. However, the stability and complexity of implementation must be carefully taken into account in the design of higher order modulators. Precise matching between the decision levels of the quantizer and the output level of the feedback D/A converter is also required for the use of multi-bit A/D converters and D/A converters.

2.2.2 Core Concept of Proposed Methodology

The key idea of this research is to tap into non-linearity and noise information about the converter contained in the sigma-delta modulator output bit stream before such information can be removed by the digital filter and decimator. This single-bit output can easily be made externally observable using one of the existing converter I/O pins using a simple gating and muxing arrangement as shown in Figure 17 below. Figure 17 describes a design-

for-test (DfT) scheme for sigma-delta A/D converters. The logic for the DfT methodology of Figure 17 rests on the observation that the digital filter-decimator is designed to mask all the non-idealities of the sigma-delta modulator to achieve the high-bit resolution that sigma-delta converters are capable of achieving. This property makes testing the sigma-delta converter difficult. This work proposes to use the information contained in the modulator output in the full-band (in-band + out-of-band) and *exploit the statistical correlation* between the *spectrum of the full-band components and the specifications of the sigma-delta A/D converter* to predict the same accurately using regression-based learning algorithms. To increase the prediction accuracy and use the low-cost test stimulus, the proposed methodology generates an optimized test input that increases the sensitivity of the sigma-delta modulator. With the increased sensitivity, the accuracy of the specifications prediction can be better and much easier than a conventional test input. As a result, the proposed methodology can test the high-precision sigma-delta A/D converters using low-cost test instrumentation. The concept of this approach is based on the alternate test methodology in [53]. In the following Chapter 2.2.3, the overview of the alternate test is briefly discussed, and Chapter 2.2.4 presents the generation of the optimized test input stimulus.

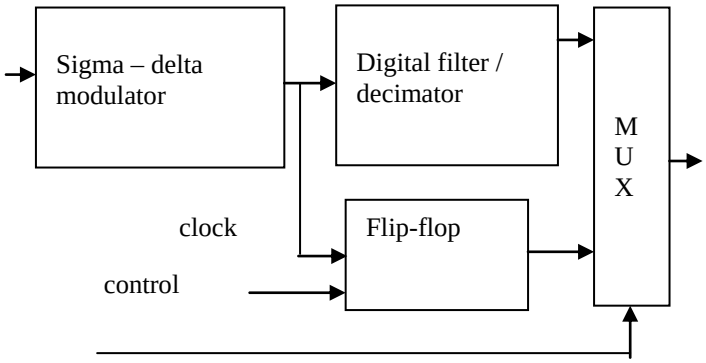

Figure 17. DfT for sigma-delta A/D converters test

2.2.3 Overview of Alternate Test

The proposed test methodology is based on the alternate test approach developed in [53], and Section 2.2.3 reviews the alternate test. The alternate test uses a statistical analysis of device output. Due to manufacturing process variations, although the devices with the same design are manufactured from the same fabrication facility, they are not exactly identical, and the specifications of the devices vary from one device to another. Target specifications or characteristics of the devices under test are initially determined in the design process, but the variations of such specifications are dependent upon the process parameter variations. If the process parameter variations are known, the specification variations are easy to be found. However, revealing the process parameter variations is not straightforward or is not possible in some applications.

The core concept of the alternate test approach is that the specifications of a device under test (DUT) may vary in a correlated manner with the measurements of the DUT, and the alternate test method builds a correlation map between the measurements and the specifications of a device under test (DUT) if such a mapping function exists. To amplify the correlation mapping, an optimized stimulus is generated to excite the DUTs. In this way, instead of revealing the process parameters variations that determine the specifications of the DUTs at a high-cost, the specifications of the DUTs can be accurately predicted from the measurements variations. This frame work in the alternate test is shown in Figure 18 that describes that the parameter variations determine the specifications of the DUTs. To achieve a low-cost test, the alternate set of measurements, which are strongly correlated to the specifications of the DUTs, can be used for predicting the specifications of the DUTs. Figure 19 presents the implementation of the alternate test approach in the proposed methodology, which uses the optimized test stimulus that excites the DUTs in a correlated manner with the measurements. Once the correlated measurements corresponding to the optimized stimulus are obtained, a regression-based algorithm builds a statistical correlation mapping function between the alternate measurements and the specifications of the DUTs. Advantages of such alternate test are as follows: (1) The approach can use the optimized stimulus that is less expensive than the required input stimulus, and (2) The approach is fast as compared to the conventional test methodology because the approach can predict all the specifications with one set of the measurements.

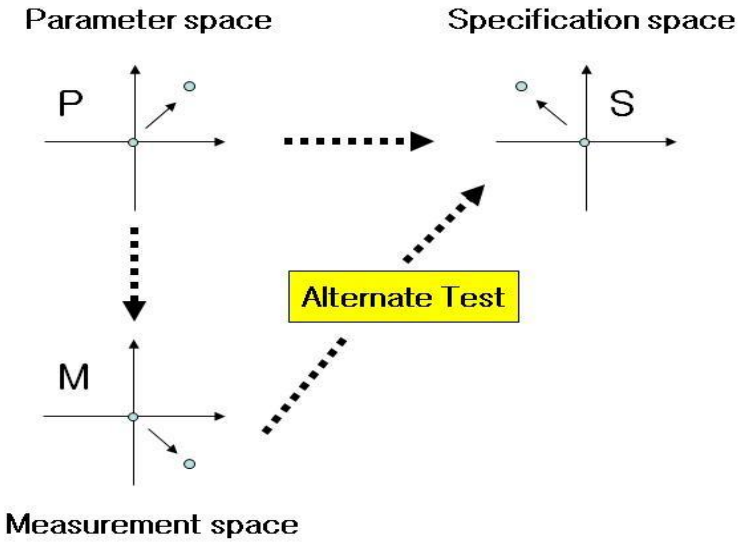

Figure 18. Alternate test frame work.

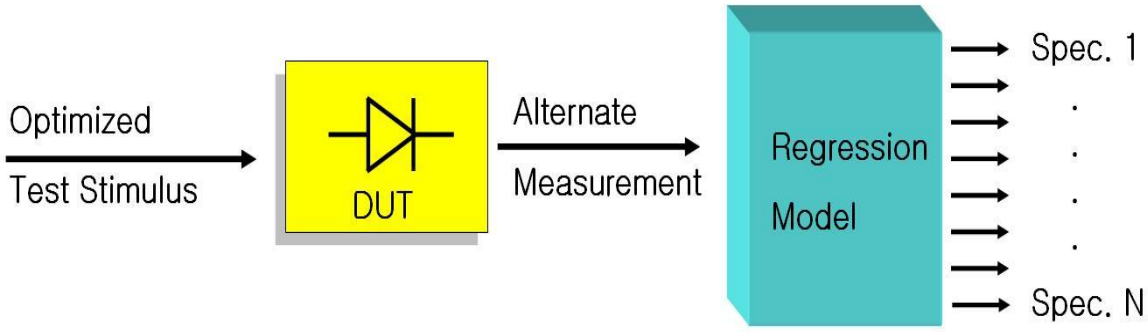

Figure 19. Implementation of alternate test approach.

2.2.4 Test Generation

As described in Section 2.2.3, the optimized stimulus must be generated to make the success of the proposed test methodology. In this thesis, the proposed methodology adopts a popular genetic algorithm [54] for the optimized test stimulus generation. The genetic

algorithm is practical and eligible for the test optimization since the genetic algorithm finds acceptable optimization solutions at a relatively fast time. Finding acceptably good solutions at acceptably fast time is beneficial in the testing area since the test techniques aim for fast and accurate approaches, which can lower the cost of testing.

Hence, the test generation algorithm that optimizes the input stimulus is a critical step in the alternate test approach to excite the sigma-delta modulator and increase the sensitivity of the output of the sigma-delta modulator. In the genetic algorithm, a structure called "*Chromosome*", which contains possible solutions of the optimization problem, evolves in the direction of better solutions from one generation to the next generation using two mechanisms called "*Crossover*" and "*Mutation*" [54]. Genetic algorithm starts with an initial population of randomly generated set of chromosomes. For each generation, the "*fitness function*" of every candidate solution is evaluated, and new chromosomes are generated. In crossover, two chromosomes are combined in a random manner defined by the crossover probability for generating new chromosomes. On the other hand, using the mutation mechanism, each chromosome is randomly varied with a certain probability to result in a new candidate solution. Furthermore, in elitism-based genetic algorithm, the best candidate solutions are propagated from one generation to the other without any change.

In the proposed methodology in this thesis, a two-tone signal is used as a test stimulus. The amplitudes and frequencies of this two-tone input stimulus are optimized in such a way that the error in the specifications prediction from the correlation mapping is minimized. The squared error between the computed specifications from the correlation map and the

known DUTs specifications summed over all the DUTs is used as a cost function for test stimulus optimization.

2.2.5 Correlation Mapping Function

With the optimized input stimulus generated by the genetic algorithm, the alternate-based test methodology requires to build the correlation mapping function to predict the specifications of the DUTs from the measurements. Chapter 2.2.5 introduces the correlation mapping function.

The correlation function maps the output or response of the DUTs to the dynamic specifications, and this mapping function is constructed from a set of training devices via a supervised learner. Among various regression techniques, the proposed methodology uses a technique called multivariate adaptive regression splines (MARS), which was developed by Jerome Friedman [55]. The MARS is a flexible technique since the MARS is a non-parametric regression technique that maps between nonlinearities and interactions and can handle both numeric and categorical data. The MARS does not limit the number of variables, which can handle either extremely little data set or extremely large data set for the accurate prediction. From a set of independent variables (measurements of the A/D converters), the MARS constructs a model to predict the dependent variables (specifications of the A/D converters).

The MARS uses a weighted sum of basis functions ($B_i(x)$) and a set of coefficients (c_i) as shown in Equation 11 to build the nonlinear regression model over a training set of the

devices under test. The number of the basis functions ($B_i(x)$) depends on the training set. Once the MARS formulate a regression equation using a set of training dataset, the regression equation is used to predict the specifications of the DUTs from the measurements of the DUTs.

$$f(x) = \sum_{i=1}^{k} c_i B_i(x) \qquad \text{Equation 11}$$

2.3. IMPLEMENTATION OF PROPOSED TEST

Previous Chapter 2.2 introduces the basic approach of the proposed methodology. In Chapter 2.3, the implementation of the proposed methodology is discussed using the concepts described in Chapter 2.2. To validate the proposed methodology in software, Section 2.3.1 provides the behavioral modeling of the sigma-delta A/D converter, and analysis of such approach is presented in Section 2.3.2. Then, Section 2.3.3 shows the simulation results to validate the proposed methodology.

2.3.1 Behavioral Modeling of Sigma-Delta A/D Converters

A second-order switched-capacitor sigma-delta A/D converter is modeled with nonlinearities in Matlab and Simulink based on [56]. The behavioral models of various sigma-delta modulators have been validated by comparing the simulation results with the

experimental hardware measurements in [56]. Main nonlinearities introduced in this model are as following:

1. clock jitter at the input sampler
2. kT/C noise in switched-capacitor circuit
3. operational amplifier DC gain
4. operational amplifier slew rate
5. operational amplifier gain bandwidth
6. operational amplifier input referred noise
7. operational amplifier saturation voltage level
8. operational amplifier total harmonic distortion
9. operational amplifier offset
10. operational amplifier PSRR

This behavioral model is a 16-bit resolution sigma-delta A/D converter, and its main parameters are summarized in Table 1. Description of the modeling is provided in the following subsections, and the final model is presented in Figure 20. Circuit diagram of a typical differential switched-capacitor integrator, which is used in the sigma-delta modulator, is also shown in Figure 21.

Table 1. Parameters of sigma-delta A/D converter behavioral model.

Parameter	Value
Bandwidth	22k Hz
Input Frequency	2.0672k Hz
Oversampling Ratio	256
Sampling Frequency	11.2896M Hz

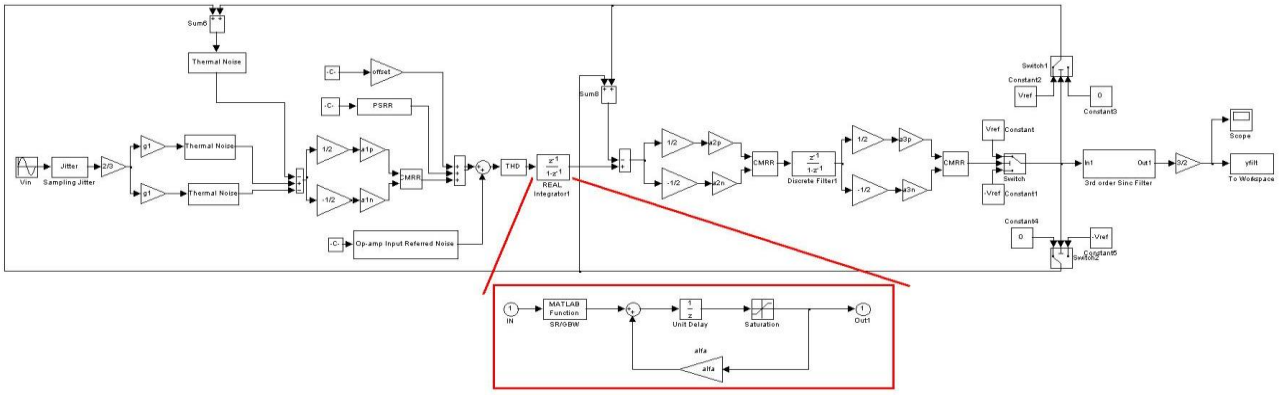

Figure 20. Behavioral model of 2nd –order differential sigma-delta A/D converter.

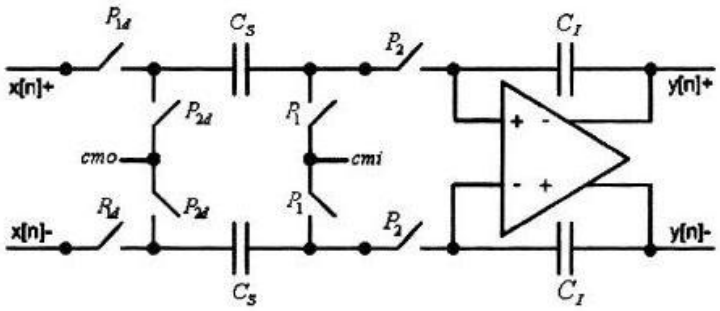

Figure 21. Typical differential switched-capacitor integrator.

2.3.1.1 Clock Jitter

The switched-capacitor circuit operates on a two-phase clock of P_1 and P_2 as shown in Figure 21, and the circuit depends on the charge transfers during each clock phase of P1 and P2. Clock jitter has effects on the sampling of an input signal only and does not give a direct effect on the switched-circuit. As a result, clock jitter introduces errors to the sampled data of the input signal. When the input signal, x(t), is a sinusoidal signal with an amplitude of A and frequency of f_{in}, the associated signal with the clock jitter error is modeled as in Equation 12 below.

$$x(t)+\delta\frac{d}{dt}x(t) \qquad \text{Equation 12}$$

A sampling uncertainty, δ, can be characterized as $\delta=\frac{1}{2\pi BW\,2^n}\sqrt{\frac{2\times OSR}{3}}$, where BW is bandwidth, n is the resolution, and OSR is oversampling ratio, which is derived from Equation 13.

$$x(t+\delta)-x(t)\cong 2\pi f_{in}\delta A\cos(2\pi f_{in}t)=\delta\frac{d}{dt}x(t) \qquad \text{Equation 13}$$

This clock jitter is assumed to be a stochastic white noise. Figure 22 shows the clock jitter model in Simulink.

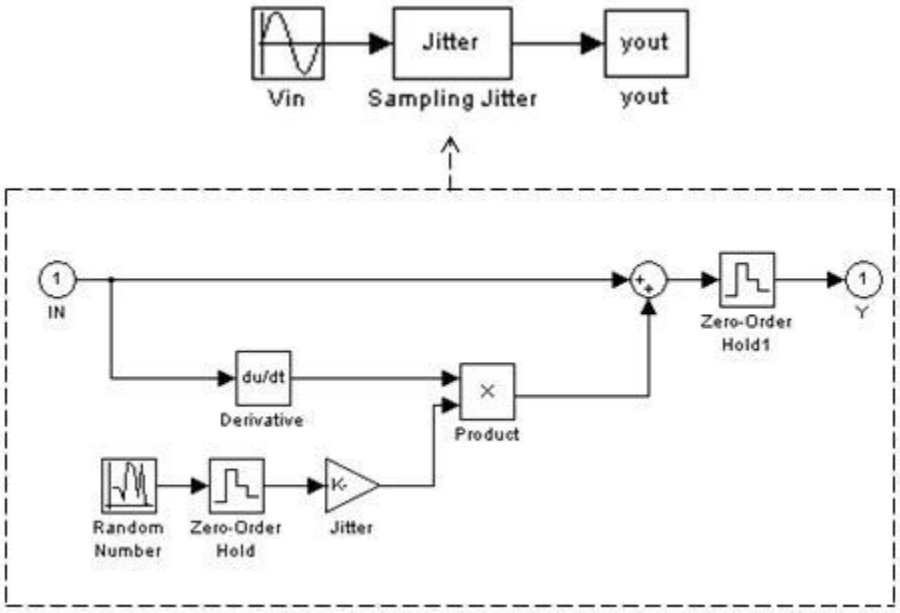

Figure 22. Clock jitter model in Simulink.

2.3.1.2 Thermal Noise

The switched-capacitor circuit consists of sampling capacitor (C_s), integrating capacitors (C_I), and switches as seen in Figure 21. When a switch is on, the MOS transistor, which is used as a switch, has a finite on-resistance (R_{on}) that introduces thermal noise. In this case, the total noise power is as follows:

$$e_T^{\,2} = \int \frac{4kTR_{on}}{1+\left(2\pi f R_{on} C_s\right)^2} df = \frac{kT}{C_s} \qquad \text{Equation 14}$$

If the input to the integrator is x(t), the switches-thermal noise can be characterized as in Equation 15.

$$Y = \left(x(t) + e_T(t)\right) \times b = \left[x(t) + \sqrt{\frac{kT}{gC_I}} n(t) \right] \times g \qquad \text{Equation 15}$$

, where n(t) is a Gaussian random process with unity standard deviation, and g is the integrator gain (C_s/C_I) . This thermal noise model in Simulink is shown in Figure 23.

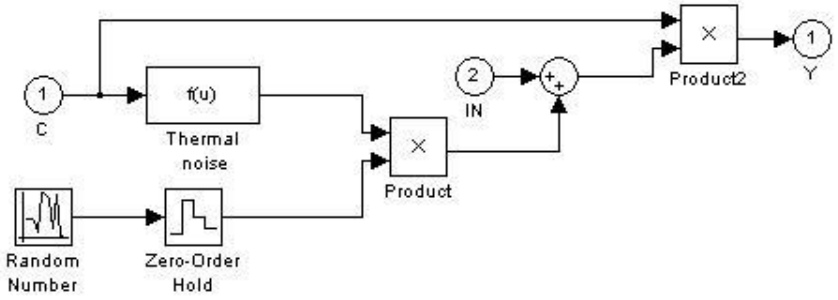

Figure 23. Thermal noise model in Simulink.

2.3.1.3 Operational Amplifier Finite DC Gain

DC gain of an ideal operational amplifier is infinity, and a z-domain transfer function of an ideal integrator is given in Equation 16 below.

$$H(z) = g \frac{z^{-1}}{1 - \alpha z^{-1}} \qquad \text{Equation 16}$$

, where g is the gain of the integrator, which is C_s/C_I, and α is a leakage factor. In the ideal case, α=1, and the feedback of the integrator has no leakage. However, the actual operational amplifier has a finite DC gain (A_o), and non-ideal transfer function is characterized as follows:

$$H(z) = \frac{C_s}{C_I}\left(\frac{1}{1+\frac{1}{A_o}\left(1+\frac{C_s}{C_I}\right)}\right)\frac{z^{-1}}{1-\left(1-\frac{C_s}{C_I}\frac{1}{A_o}\right)z^{-1}}$$ Equation 17

This non-ideal transfer function reveals that the finite DC gain introduces not only the leakage in the integrator feedback but also introduces the reduced gain. Consequently, a fraction of this leakage of the previous output of the integrator is added to each new input sample of the integrator. Note that the leakage factor α is 1- $C_s/(C_IA_o)$ instead of 1 ideally. Figure 24 shows the integrator models in an ideal case (left) and a non-ideal case (right). As shown in Figure 24, the non-ideal integrator introduces the leakage in the feedback.

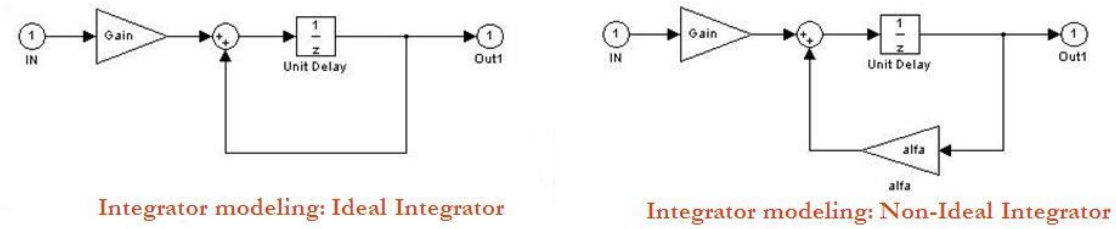

Figure 24. Finite DC gain model in Simulink: integrator with infinity DC gain in left and non-ideal integrator with finite DC gain in right.

2.3.1.4 Slew Rate and Gain Bandwidth

Slew rate is the maximum rate of a signal change and dictates the non-linear settling section. Slew-rate limit occurs when the amplifier cannot supply sufficient current to the output, and consequently, a wrong value of charge can be transferred to the feedback capacitance. Gain bandwidth is the product of the closed-loop gain and 3dB bandwidth, and

its value for the ideal op amp is infinity. Slew rate, gain bandwidth, and finite DC gain are all related to each other. Its modeling is as follows:

During integration period when P_2 is on between ($nT_s - T_s/2$) and nT_s, the evolution of the integrator output is $v_o(t) = v_o(nT_s - T_s) + \alpha \times v_{in}(nT_s - T_s/2)(1 - e^{-t/\tau})$, where v_{in} is the input to the integrator, α is the leakage due to finite DC gain, and τ is a time constant, where $\tau = 1/(2\pi GBW)$. Above output has the maximum slope of $\left|\frac{d}{dt}v_o(t)\right|_{\max} = \alpha\frac{v_s}{\tau}$, where $v_s = v_{in}(nT_s - T_s/2)$. As a result, if the above maximum slop is less than the slew rate limit, no slewing occurs. In contrast, when slew rate exceeds the maximum slop, the circuit is in slewing under following conditions:

1. $v_o(t) = v_o(nT_s - T_s) + SR \times t$ if $t_{\max} \le t_o$
2. $v_o(t) = v_o(t_o) + (\alpha V_s - SR \times t_o) \times \left(1 - e^{-\frac{t-t_o}{\tau}}\right)$ if $t_{\max} > t_o$

, where $t_o = \frac{\alpha V_s}{SR} - \tau$ and $t_{\max} = \frac{T_s}{2}$

Figure 25 describes the Simulink model for the slew rate and gain bandwidth. Above mathematical formulations with the conditions are written and performed in Matlab code function as shown in Figure 25 depending on the input value to the integrator.

2.3.1.5 Saturation Level

The operation of the operational amplifier depends on the value of saturation limit. Output voltage swing of the amplifier is linearly proportional to the difference between input terminals in operation range, but it is limited by the power supply, called amplifier

saturation. Whenever the output voltage reaches the saturation limit value, the voltage is clipped and cannot exceed the limit. The saturation level is expected to be close to the power supply rails, but it is smaller than power supply in general. This saturation level determines the dynamic range of the amplifier. To take this dynamic range of signals in the modulator into account, the saturation level must be modeled, and Simunlink provides the saturation block that limits the signal values. The saturation model is also shown in Figure 25.

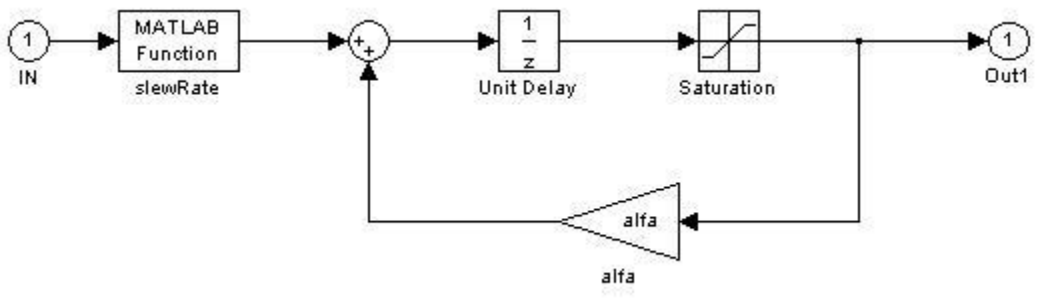

Figure 25. Slew rate, gain bandwidth, and saturation level in Simulink.

2.3.1.6 Input Referred Noise

Total RMS noise voltage of the operational amplifier referred to the integrator input is called input referred noise. This noise can be easily modeled at the integrator input with available Gaussian distribution, zero mean, and unity standard deviation in Simulink. This noise can be added to the integrator input signal. If the input to integrator is x(t), then this input becomes $x(t) + V_{rms\text{-}Gaussian}$.

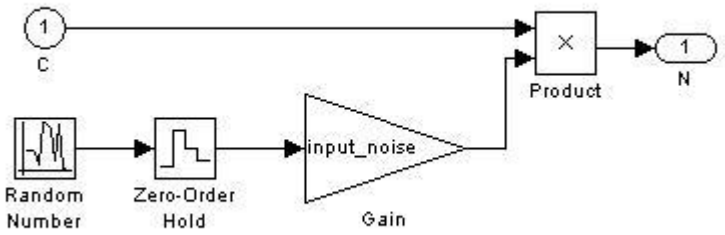

Figure 26. Input referred noise model in Simulink.

2.3.1.7 Input Bias

Ideally, the operational amplifier should have a zero input voltage when the differential input terminals are shorted (V+=V-), and the output is a virtual ground. However, the operational amplifier includes a leakage or bias current into the amplifier in real world, which generates an offset voltage. This offset voltage is caused by input mismatches or imperfections in the differential amplifier. The offset value is added to the input signal to the integrator and is shown in Figure 27.

2.3.1.8 Power Supply Rejection Ratio (PSRR)

PSRR describes the noise amount from a power supply that the operational amplifier can reject. This PSRR is defined as a ratio of the change in supply voltage to the corresponding change in output voltage as seen in Figure 18.

$$PSRR = \frac{\Delta V_{supply}}{\Delta V_{out}} \qquad \text{Equation 18}$$

The power supply affects bias point of differential input pair of the operational amplifier, and hence PSRR is modeled as another source of offset at the input. PSRR model in Simulink is shown in Figure 27.

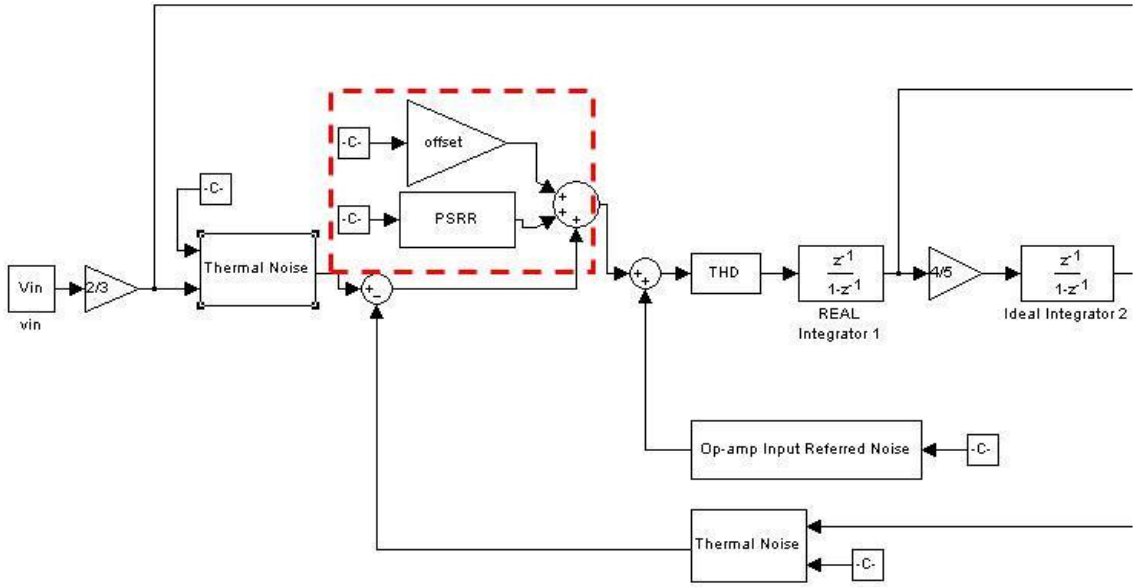

Figure 27. Input bias and PSRR model in Simulink.

2.3.1.9 Total Harmonic Distortion

Total harmonic distortion (THD) is a measure of the harmonic power contents injected into a sinusoidal signal due to distortion. It is defined as a ratio of the sum of harmonic powers to the power of the fundamental frequency. Since the poor THD performance of the operational amplifier introduces distortions and degrades the device performance, its effect must be taken into account. Output voltage swing and slew rate are two main factors for distortion in the operational amplifier. In general, only first 5 harmonics are significant and

considered, and the THD with first fundamental and 2 harmonics is modeled for simplicity. When the input to the integrator is x(t), the signal with THD can be modeled as follows:

$$y(t) = \alpha_1 x(t) + \alpha_2 x(t)^2 + \alpha_3 x(t)^3 \qquad \text{Equation 19}$$

The coefficients of the α_i (i=1, 2, 3) in Equation 19 are determined in simulation to generate the proper THD. Figure 28 shows its Simulink model.

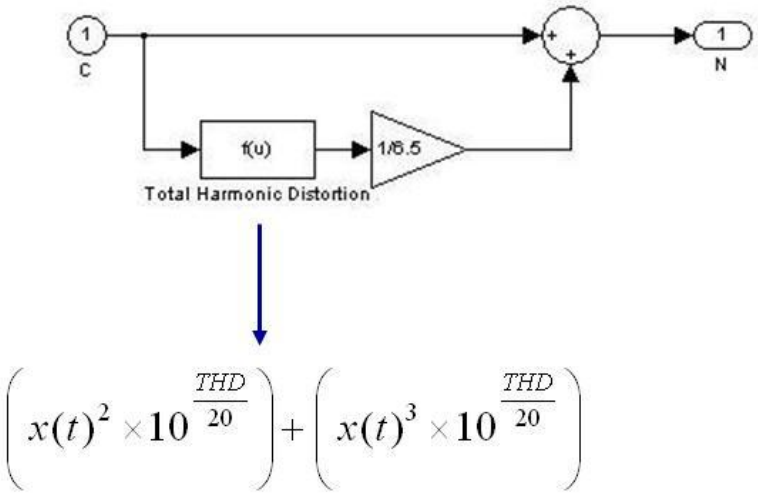

Figure 28. THD model in Simulink.

2.3.2 Analysis of Proposed Methodology

Section 2.3.2 presents the analysis of the proposed methodology using the concepts given in Chapter 2.2. The test stimulus using the genetic algorithm is generated in Section 2.3.2.1, and the sensitivity analysis of the sigma-delta modulator corresponding to the optimized test input is provided in Section 2.3.2.2.

2.3.2.1 Test Generation

As described in Chapter 2.2, the test generation is required in the proposed test methodology. The optimized test stimulus must be generated in such a way that the stimulus increases the sensitivity of the sigma-delta A/D converters for the regression-based mapping algorithm (MARS) to construct an accurate correlation between the measurements and the specifications of the sigma-delta A/D converters.

In this research work, a two-tone sinusoidal input signal is generated using the genetic algorithm to stimulate the DUTs. Figure 29 presents the performance of the genetic algorithm. In Figure 29, the genetic algorithm reduces the fitness function at every generation from its initial value as the algorithm reaches an optimization point. As seen in Figure 29, the genetic algorithm converges to the best solution (the optimization point) after 35 generations. The amplitudes and frequencies of the optimized two-tone signal are summarized in Table 2. In summary, the genetic algorithm has improved the solution almost 39 times better than the initial solution and also improved the mean fitness value about 49 times from its initial mean fitness value. The result proves the effectiveness of the genetic algorithm. Such optimized two-tone sinusoidal stimulus is applied to the high-precision sigma-delta A/D converters under the test.

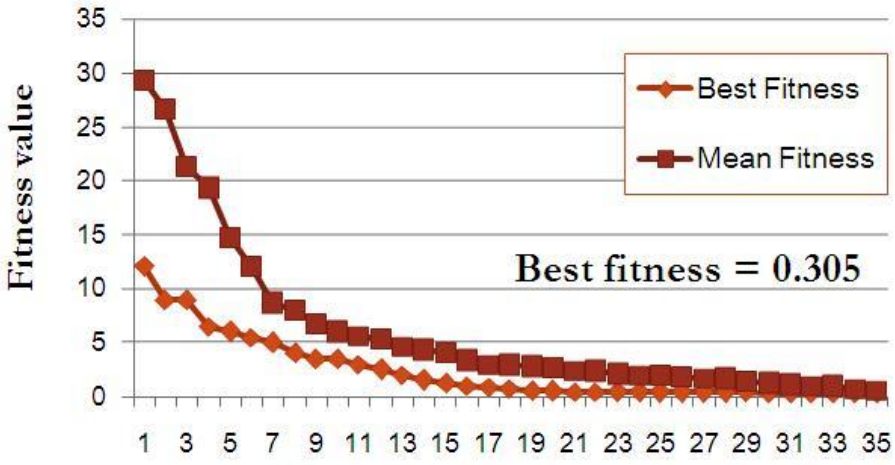

Figure 29. Genetic algorithm performance

Table 2. Optimized two-tone signal parameters

	First Tone	Second Tone
Amplitude (V)	0.4897	0.8640
Frequency (kHz)	0.844	2.530

2.3.2.2 Sensitivity Analysis

Based upon the information generated by the genetic algorithm in Section 2.3.2.1, the two-tone signal is applied to the sigma-delta A/D converters. As described in Chapter 2.2, the proposed test methodology makes the use of the modulator output (full-band spectrum) instead of the output from the sigma-delta A/D converters (in-band spectrum). This Section

2.3.2.2 analyzes the sensitivity of the converters using the optimized stimulus, which shows practicability of the proposed methodology.

2.3.2.2.1 Single-tone stimulus versus optimized two-tone signal

Section 2.3.2.2.1 investigates the sensitivity analysis of a single-tone input signal versus an optimized two-tone input signal. This sensitivity analysis shows the usefulness of the optimized two-tone input signal generated by the genetic algorithm. The comparison of DUT harmonic powers using the single-tone input signal and the optimized two-tone input signal is shown in Figure 30. The dynamic range of the total harmonic power for the two-tone signal is 20dB as compared to 10dB for the single-tone signal. This argues in favor of using the two-tone signal as the test input to the modulator as opposed to the single-tone signal.

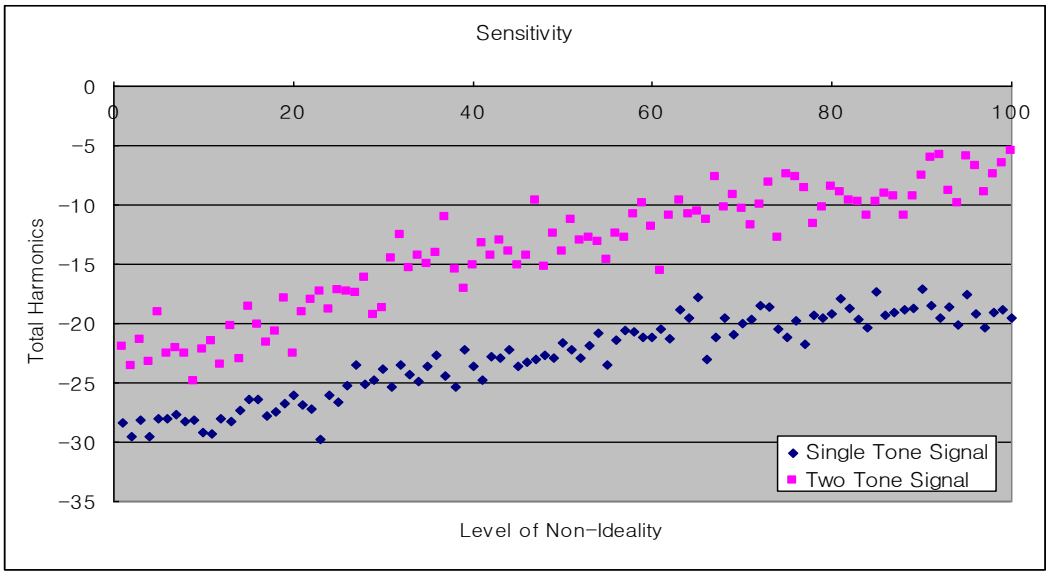

Figure 30. Harmonic power versus device nonlinearity.

2.3.2.2.2 In-band versus full-band

The usefulness of an access to the full-band spectrum is illustrated in Figure 31 and Figure 32. Figure 31 shows the dynamic range of the in-band noise power, and Figure 32 shows the dynamic range of the full-band noise power. In both Figure 31 and Figure 32, the noise power of the sigma-delta modulator is increased by scaling all the noise sources in the model of Figure 20. The in-band noise power is computed and shown against the intrinsic noise of the converter in Figure 31, and that is what would be measured at the output of the filter/decimator of the converter if the scheme of Figure 17 were not used. Figure 32 shows the full-band noise power versus the same intrinsic noise of the converter as measured by the analysis of the sigma-delta modulator bit stream. Note that the dynamic range of the full-band noise power in Figure 32 is 50dB, while the dynamic range of the in-band noise power in Figure 31 is much smaller than the case of the full-band noise power, which is 35dB dynamic range for the in-band noise power. This significantly increased sensitivity of the test measurement to the intrinsic noise of the sigma-delta modulator allows reduction in the cost of test instrumentation and the reduction in test time. This aspect proves that the modulator output information is more useful with the optimized two-tone test stimulus than the A/D converter output. This useful information would be masked by the digital filter and decimation when the output of A/D converters is used.

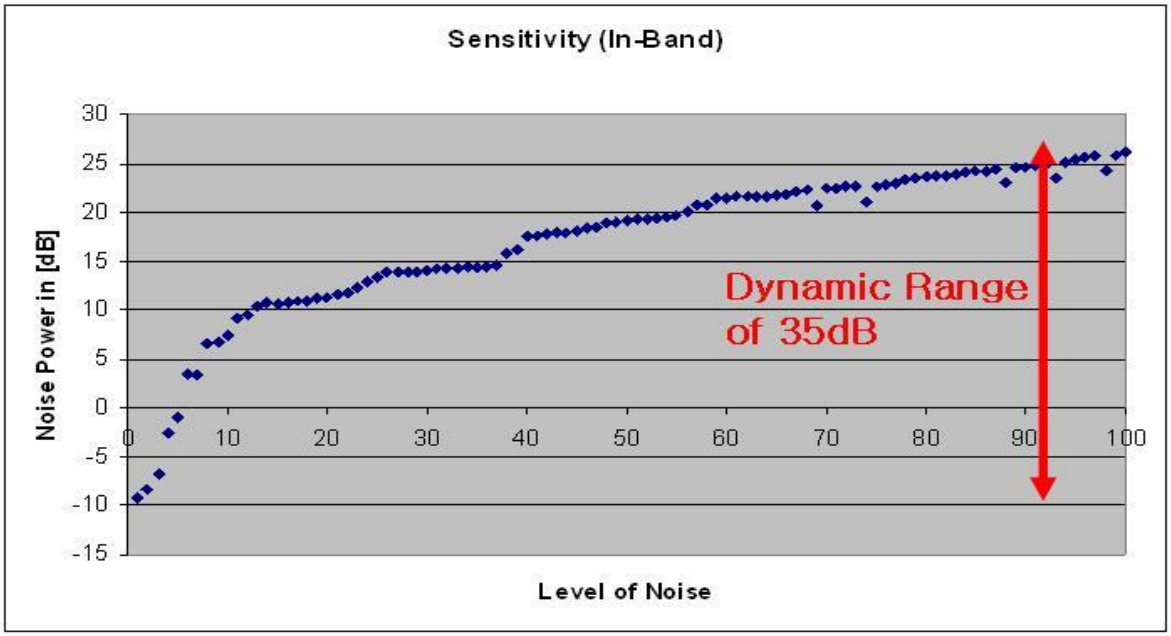

Figure 31. In-band noise power versus intrinsic noise level

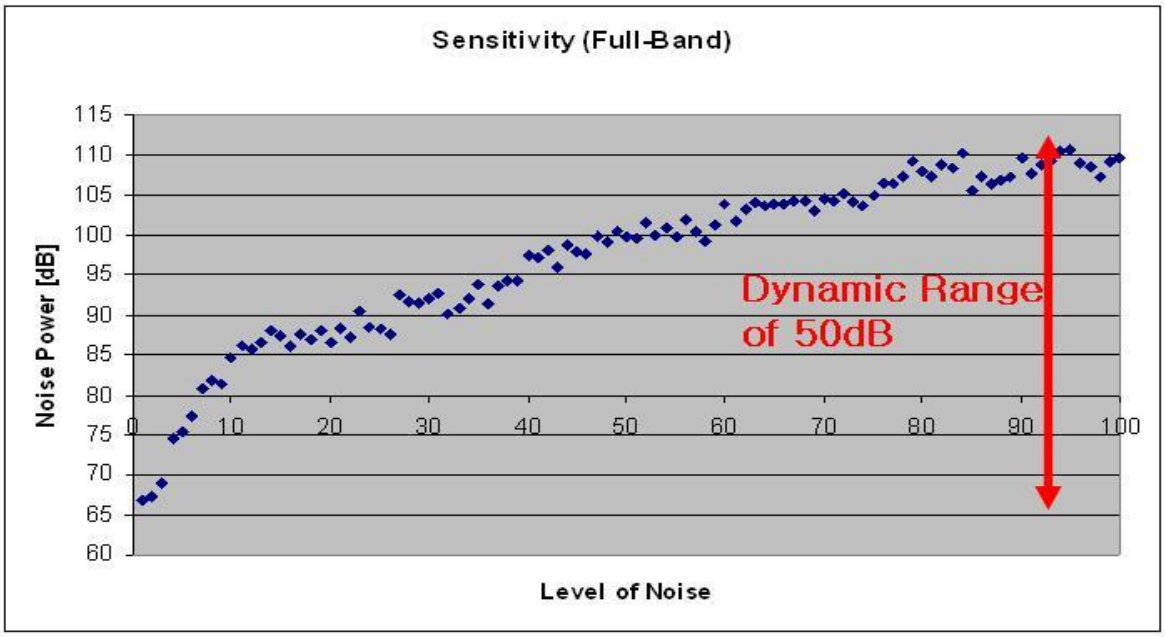

Figure 32. Full-band noise power versus intrinsic noise level

2.3.2.2.3 Effects of nonlinearity

The sensitivity described in above Figure 30 - Figure 32 are further corroborated in this Section 2.3.2.2.5. Figure 33 presents the effects of the nonlinearities shown in the full-band when the optimized two-tone test stimulus is applied to the sigma-delta A/D converters under test. In this Figure 33, the nonlinearity values are varied by 30% from the nominal values. It is seen that each of nonlinearity affects the power spectrum density in a different way. For example, the slew rate produces lots of odd harmonics, while the noise increases the noise floor and removes the noise property. In addition, such effects of the nonlinearities can be hidden at the output of A/D converters since such effects are removed by the digital filter and decimator filter.

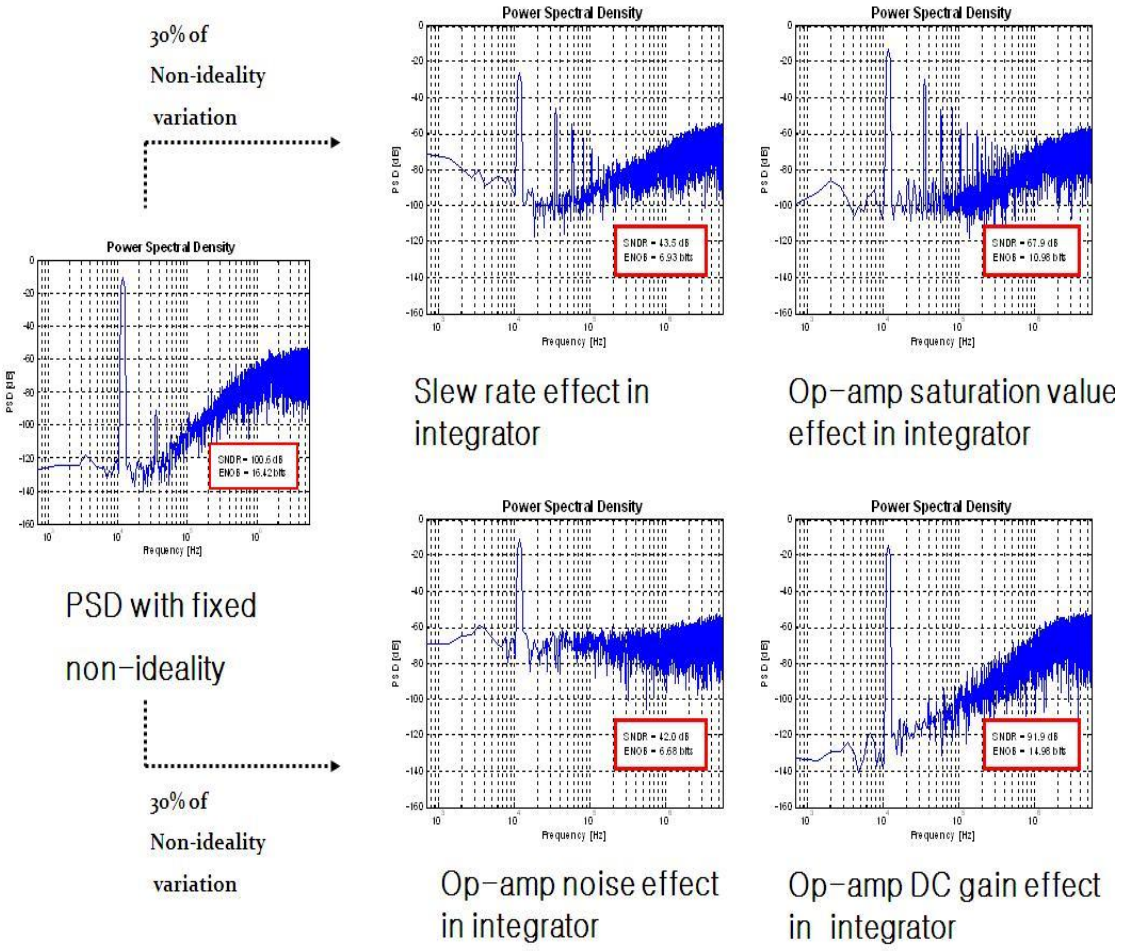

Figure 33. Effects of nonlinearities

Figure 34 and Figure 35 show the spectra for two different op-amp slew rates and saturation values respectively as an example. In both, the out-of-band harmonics are impacted significantly by the non-linearity introduced into the device. Further, different levels of such nonlinearities impact differently.

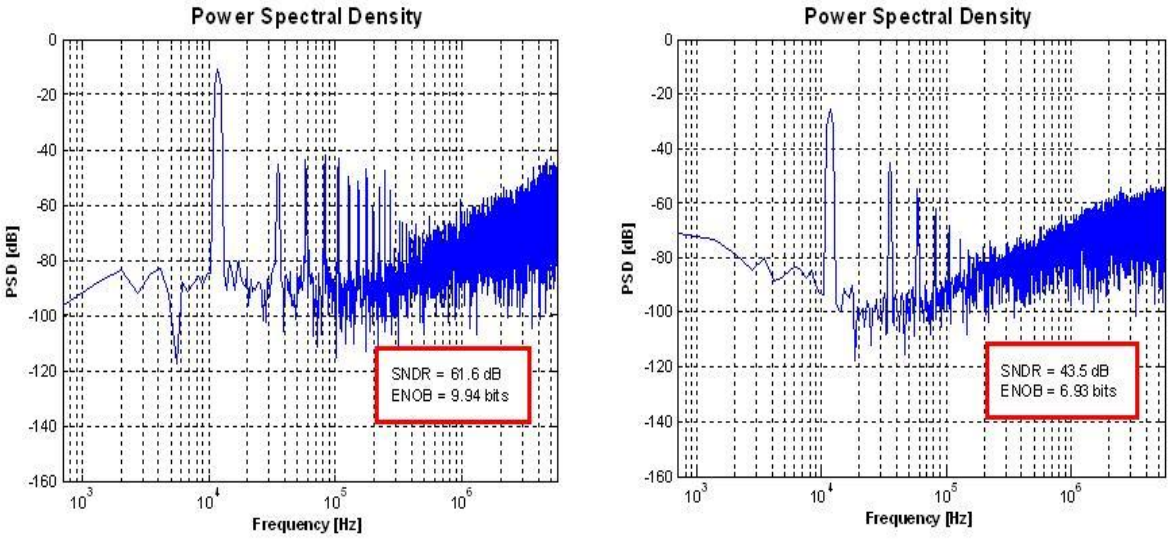

Figure 34. Effects of op-amp slew-rate variations

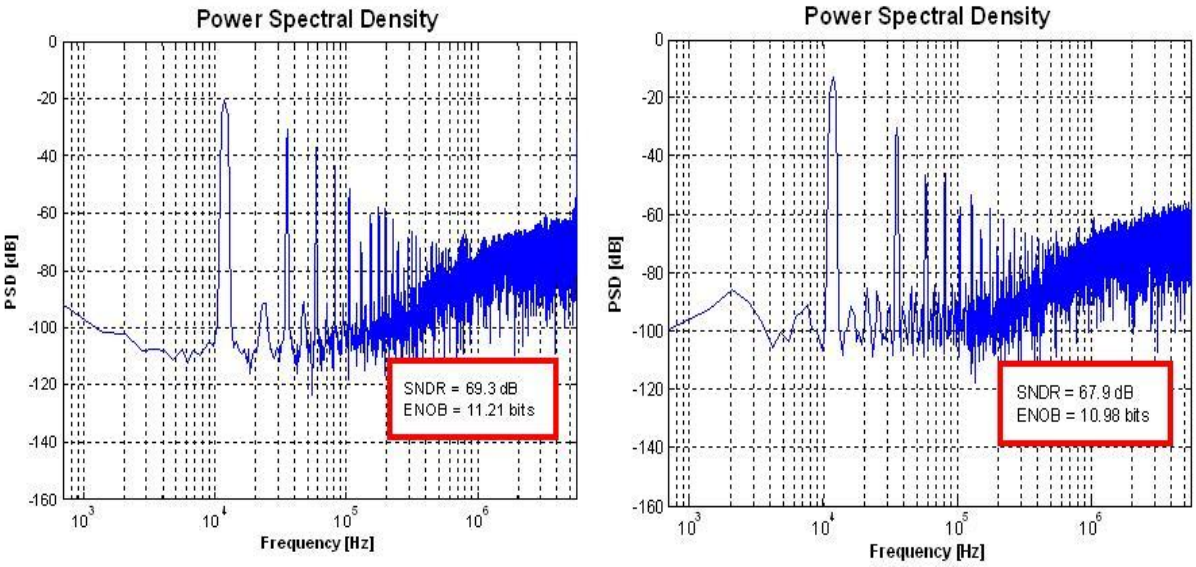

Figure 35. Effects of op-amp saturation variations

2.3.2.2.4 Correlation between each specification

In addition to the previous sensitivities and effects of the nonlinearities, correlations between each specification help the regression mapping algorithm (MARS) build a strong correlation map between the measurements and the specifications. Figure 36 - Figure 38 demonstrate the correlations between the ENOB, SNR, and THD specifications of the sigma-delta A/D converters. Since all the ENOB, SNR, and THD specifications of the sigma-delta A/D converters are a measure of a signal power, noise power, and/or harmonic distortions, they are strongly correlated. Hence, the proposed methodology of building a correlation map between the specifications and measurements for the test purpose is attractive.

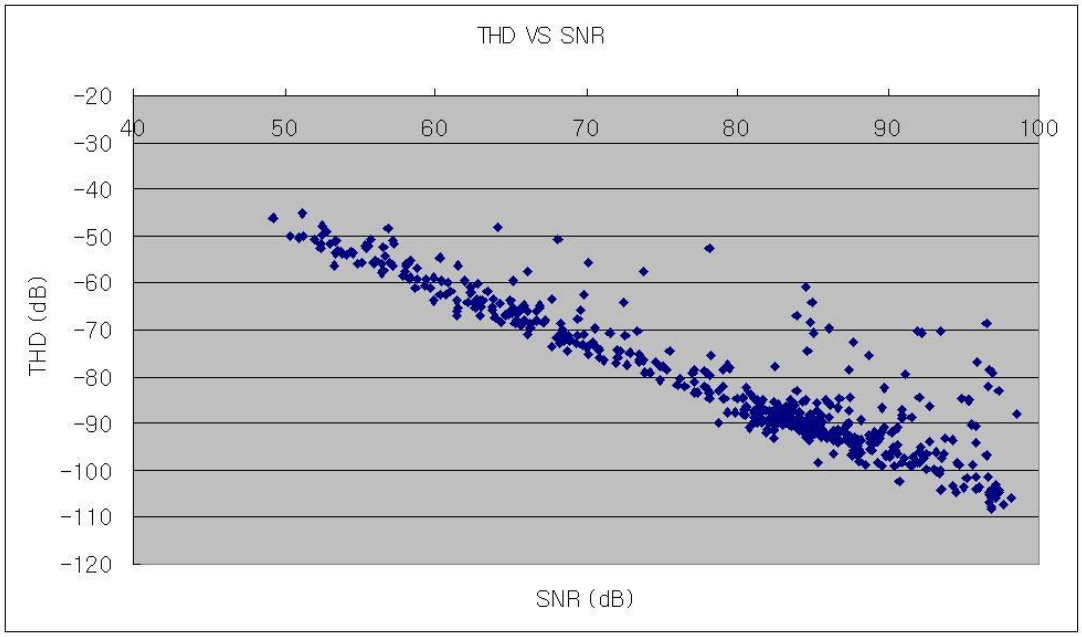

Figure 36. SNR versus THD plot for 500 devices

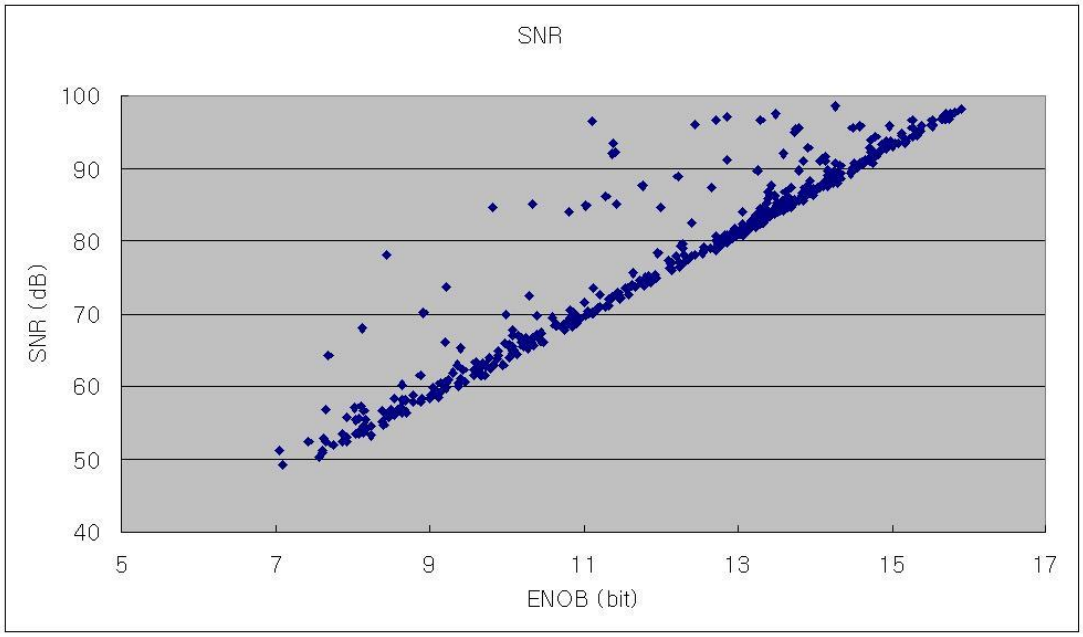

Figure 37. SNR versus ENOB plot for 500 devices

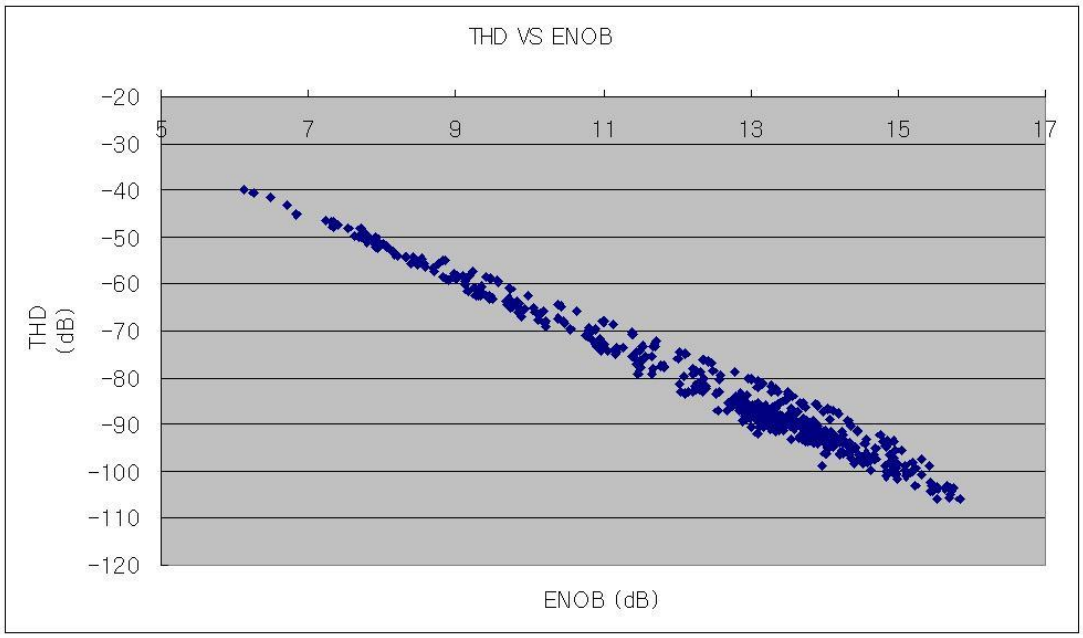

Figure 38. THD versus ENOB for 500 devices

2.3.3 Simulation Results for Validation

In computer simulation, the specification predictions using the proposed low-cost dynamic test methodology were evaluated and validated. Using Matlab and Simulink (Mathworks, Inc.), 500 instances of the sigma-delta A/D converters were implemented based on the behavior model described in Section 2.3.1 with intentionally induced performance variations assuming random process variations. The specifications (ENOB, SNR, and THD) of each device under test were predicted using 10 cycles of a two-tone stimulus based on (1) the proposed full-band spectrum analysis method (output of the modulator), (2) analysis of only the in-band spectrum (output of the converter), and (3) the conventional methodology (FFT analysis of the converters output). The predicted specification values for the 500 instances, obtained from the three different test methods, were compared to each other. In summary, the proposed full-band spectrum-based method shows better predictions compared to the other two methodologies, especially in the case of using the low-resolution test stimulus, according to the simulation results.

Figure 39 shows three plots for ENOB (left), SNR (middle), and THD (right) when the devices are tested with a 14-bit input signal using the proposed methodology and the conventional methodology. Each graph shows the corresponding specification values predicted from the full-band spectrum of the output of the modulator (methodology proposed in this paper) on the y-axis versus the actual value of the specification on the x-axis. Two plots are shown in each graph. One plot is based on the full-band spectrum data as discussed above. The other plot is based on computation of the specification value from

Fourier analysis of the converters output (conventional test method). The measurement results using the conventional test method were not accurate for the data converters that have high ENOB, SNR, and THD since the 14-bit linearity input stimuli were applied to the DUTs.

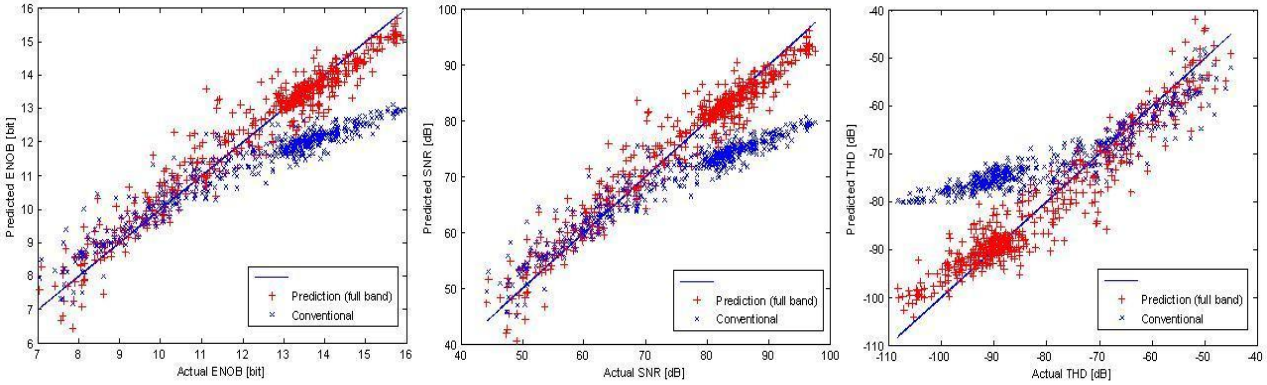

Figure 39. Proposed method predictions from full-band data and conventional method measurements using 14-bit input stimuli.

Figure 40 presents the results using lower linearity test stimuli than the above 14-bit test stimuli. Figure 39 and Figure 40 differ only in the aspect that the 16-bit A/D converters under test were tested using the 14-bit accuracy stimulus in Figure 39 versus 12-bit accuracy stimulus in Figure 40. Note that the full-band-based prediction plot is more linear compared to the one with the conventional method, where measurement noise is dominant especially for the instances with low-noise and low-distortion.

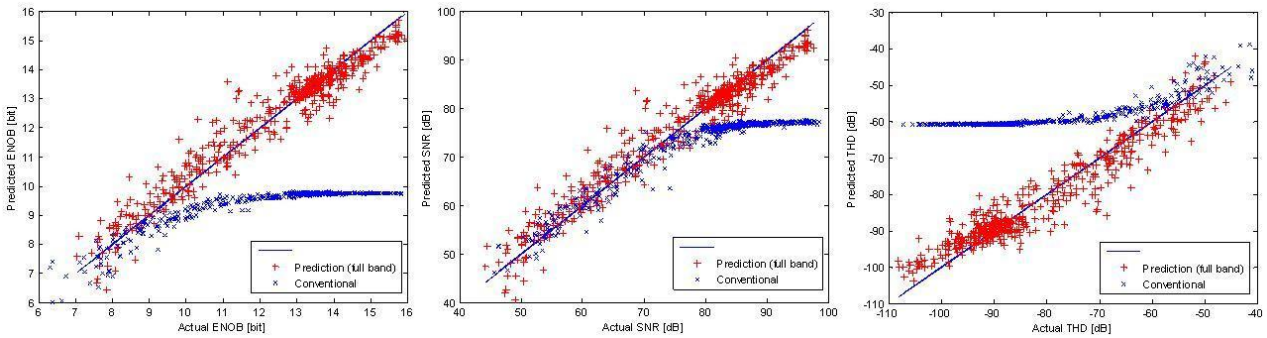

Figure 40. Proposed method predictions from full-band data and conventional method measurements using 12-bit input stimuli.

For comparison, in-band-spectrum-based prediction results are shown in Figure 41, Figure 42, and Figure 43. As shown in Figure 41 - Figure 43, the predictions of the specifications for the 500 devices using the full-band information were much better than the predictions using the in-band information.

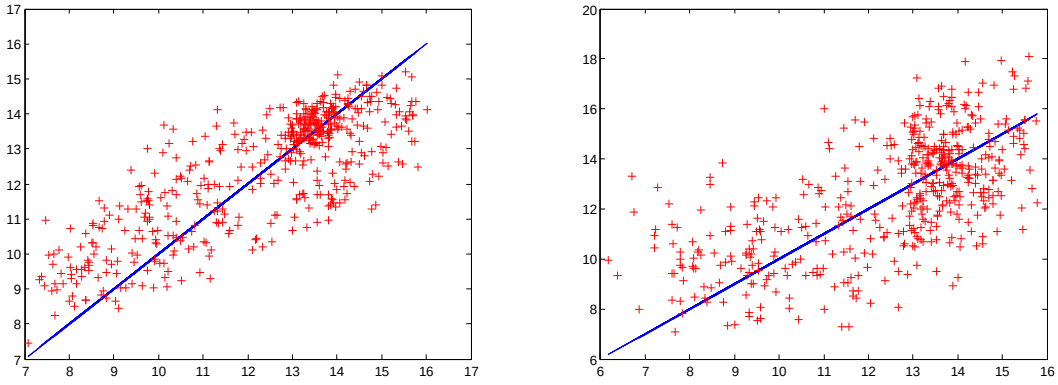

Figure 41. ENOB predictions from in-band data:
(a) 14-bit input (Left). (b) 12-bit Input (Right).

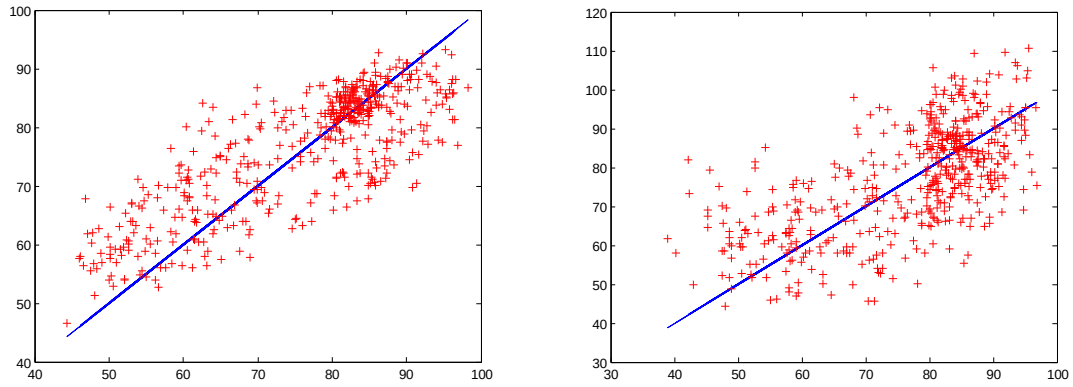

Figure 42. SNR predictions from in-band data:
(a) 14-bit input (Left). (b) 12-bit Input (Right).

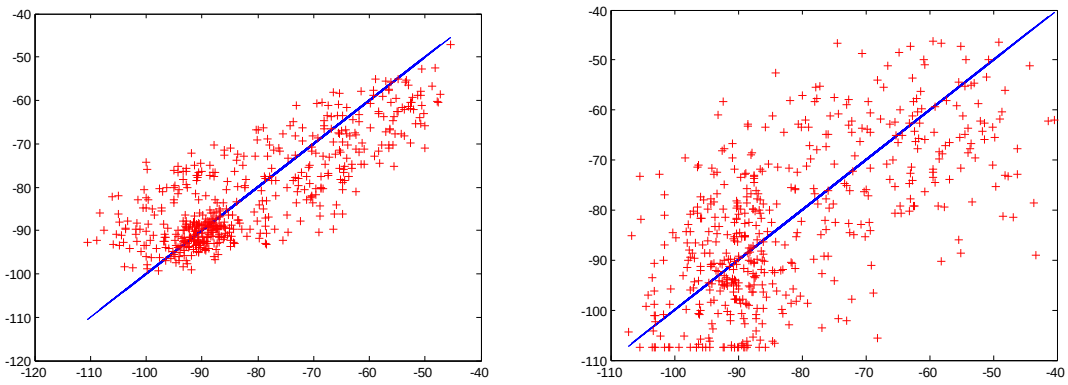

Figure 43. THD predictions from in-band data:
(a) 14-bit input (Left). (b) 12-bit Input (Right).

In above simulations, the 16-bit sigma-delta A/D converters were tested by applying lower resolution input signals, which are 14-bit resolution and 12-bit resolution. In Figure 44, Figure 45, and Figure 46, ENOB, SNR, and THD were predicted using a 20-bit accuracy input stimulus from full-band spectrum. The 20-bit input signal is a required resolution for testing the 16-bit A/D converters with the conventional test method. The

predictions results using 20-bit resolution signal become better, but the results are not extremely superior compared to the results using the 14-bit resolution input signal, which is a low-cost signal. Generation of such 20-bit resolution signal source is extremely expensive, far exceeding the cost of 14-bit resolution signal source. This concludes that the proposed methodology with the low-cost test instrument of 14-bit input signal is a good candidate for testing high-resolution sigma-delta A/D converters.

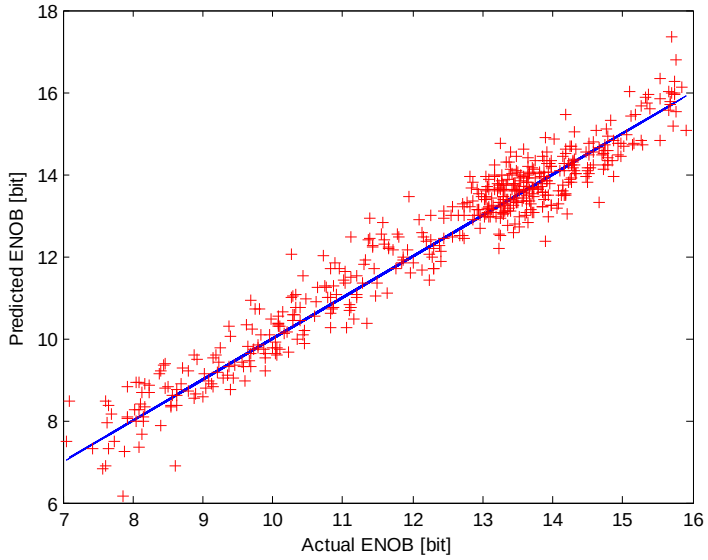

Figure 44. ENOB predictions (repeatability) from full-band using 20-bit Input.

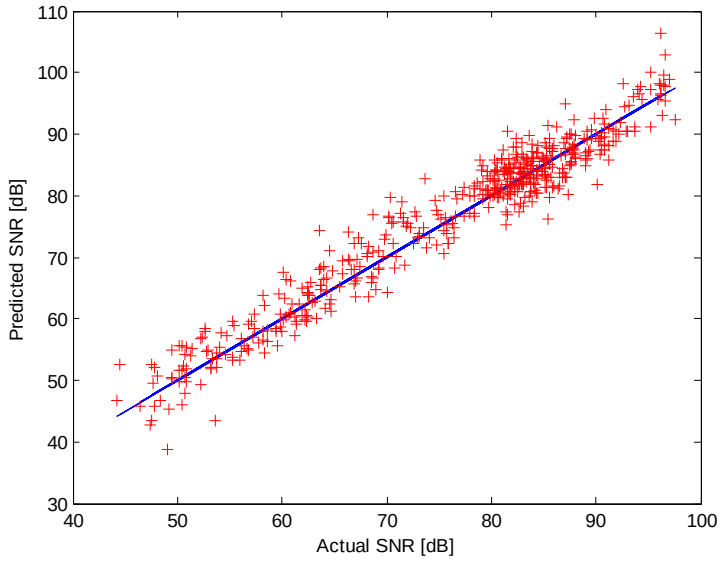

Figure 45. SNR predictions (repeatability) from full-band using 20-bit Input.

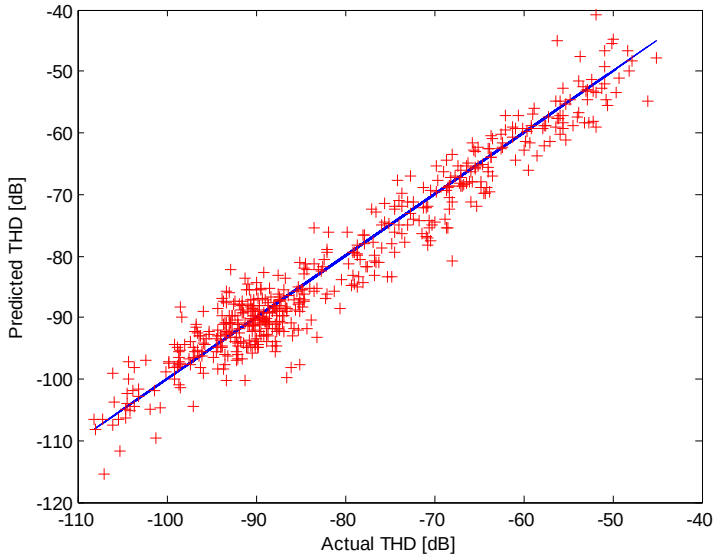

Figure 46. THD predictions (repeatability) from full-band using 20-bit Input.

The comparisons of test results using all of the above cases are summarized in Table 3. The prediction error values are greater than those of the full-band-based prediction in all test cases.

Table 3. Specifications prediction errors (RMS).

Specifications	Stimulus Resolution	Full-Band	In-Band	Conventional
ENOB	20	0.5320	0.6313	0.4938
	14	0.5376	1.5436	1.4413
	12	0.5420	1.9469	3.4363
SNR	20	3.2025	3.8007	2.9727
	14	3.2366	8.2710	8.6767
	12	3.2532	11.7210	9.6597
THD	20	3.7628	4.4012	3.4868
	14	4.3790	10.5231	13.1688
	12	4.5514	13.1164	20.8730

2.4. VALIDATION OF PROPOSED TEST

The proposed test methodology for the dynamic specifications of the sigma-delta A/D converters has been validated by performing the hardware experiment. The Chapter 2.4

presents the experimental test setup and test procedure in Section 2.4.1, and then, the results of the experiments are discussed in Section 2.4.2.

2.4.1 Test Setup

Since the methodology proposes a design-for-test (DfT) scheme that requires an access to the output of the sigma-delta modulator, and the specifications of the devices under test (DUTs) must have small and large variations (good DUTs and defective DUTs), the hardware experiment was not easy with commercially available sigma-delta A/D converters. Therefore, the sigma-delta modulator has been designed and built on a printed circuit board (PCB). For simplicity and due to the lack of high-performance test-measurement equipment, a first-order sigma-delta modulator has been chosen. To vary the nonlinearities of the sigma-delta modulator as a result of process parameters in this experiment, the modulator on PCB includes a socket for an eight-pin dual in-line package (DIP) type, and various commercial operational amplifiers (OP AMPs) with different performances, which are also packaged in the eight-pin DIP, sit on the socket instead of injecting nonlinearities into the sigma-delta modulator. The designed first-order sigma-delta modulator is presented in Figure 47. The sigma-delta modulator consists of one operational amplifier, a LM2903 comparator from National Semiconductor, a 74HC74 positive-edge D-type flip-flop from Texas Instruments, and a SN74AHCT1G125 buffer from Texas Instruments. For the operational amplifier in the integrator of the modulator, 14 different models were used, and

these operational amplifiers are summarized in Table 4. Total number of the operational amplifiers used in this experiment is 60.

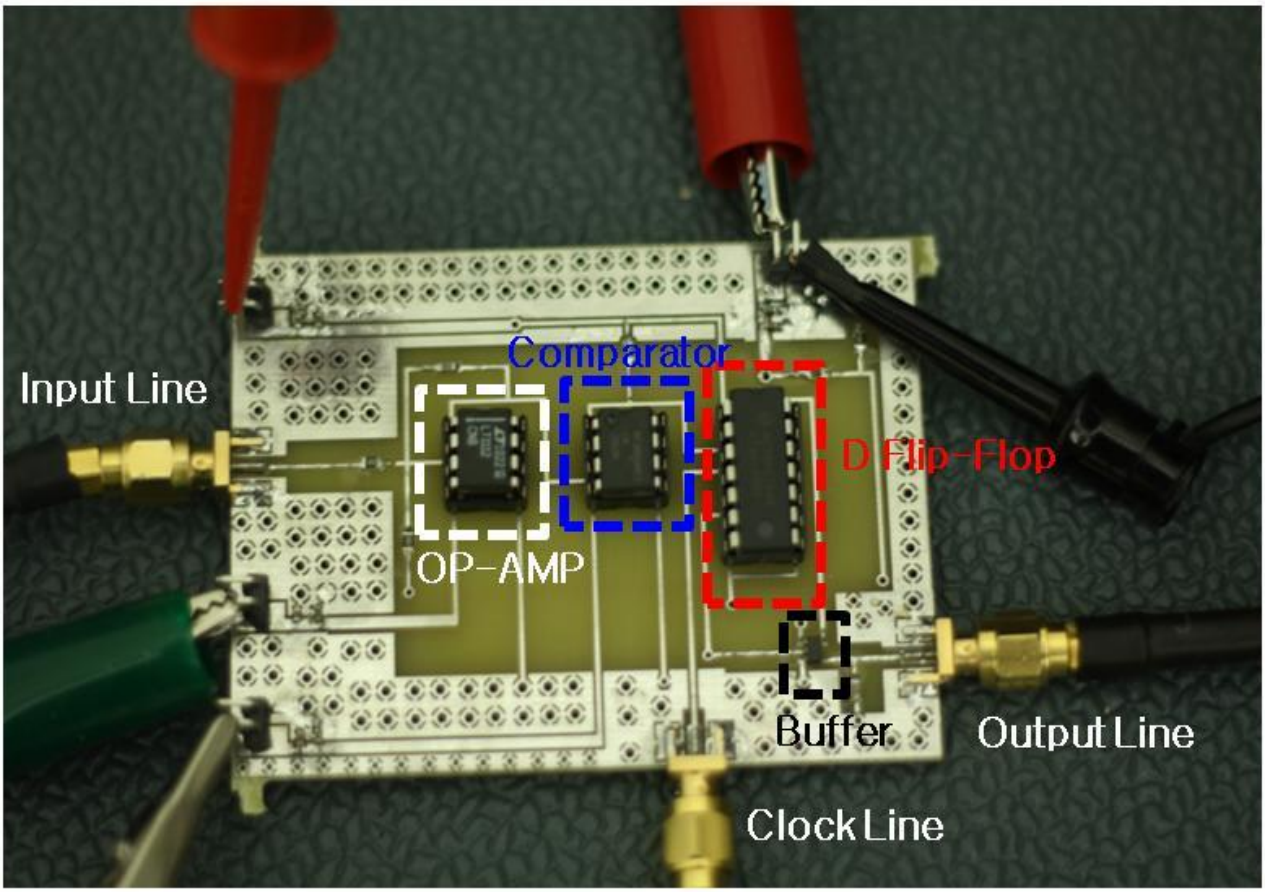

Figure 47. First-order sigma-delta modulator.

Table 4. Summary of operational amplifier

Manufactures	Part number	Quantity
Linear Technology	LT1490	2
	LT1013	2
	LT1413	2
	LT1112	2
	LT1211	2
	LT1113	2
	LT1169	2
Analog Devices	AD712	2
	AD822	2
	AD648	2
Texas Instruments	MC1458	10
	LF353	10
	TLV2362	10
	LM833	10

A sinusoidal input signal with an amplitude swing of 0V to 5V and an input frequency of 1.4648k Hz was generated using a 14-bit resolution arbitrary waveform generator (AWG), Agilent 33220A, and fed into the input signal line of the PCB shown in Figure 47. A clock source of 1MHz was generated using Tektronix AFG320 and applied to the D-type flip-flop and a 14-bit digitizer ATS460 from AlazarTech to oversample the input signal of the modulator and synchronize the data acquisition. The output data of the sigma-modulator was acquired using the digitizer ATS460, and example plots of the 1-bit data stream from the sigma-delta modulator output and its power spectrum density (PSD) plot using AD712 operational amplifier are shown in Figure 48 and Figure 49, respectively. The total number of samples collected was 8192, and the number of cycles was 12, which satisfies the coherent sampling condition.

The sigma-delta A/D converter consists of the sigma-delta modulator and a digital filter. In the hardware experiment, once the output data of the sigma-delta modulator is acquired into a computer, this output must go through the digital filter. This digital filter is implemented in software (Matlab) to reconstruct the digital signal and remove the noise in the high-frequency band. A finite impulse response (FIR) low-pass filter (LPF) was chosen as the digital filter. Figure 50 presents a comparison between the FFT plot of the sigma-delta modulator output, which is before the digital filter and used in the proposed methodology, and the FFT plot of the sigma-delta A/D converter, which is a filtered version of the modulator output. The overall test measurement setup is shown in Figure 51.

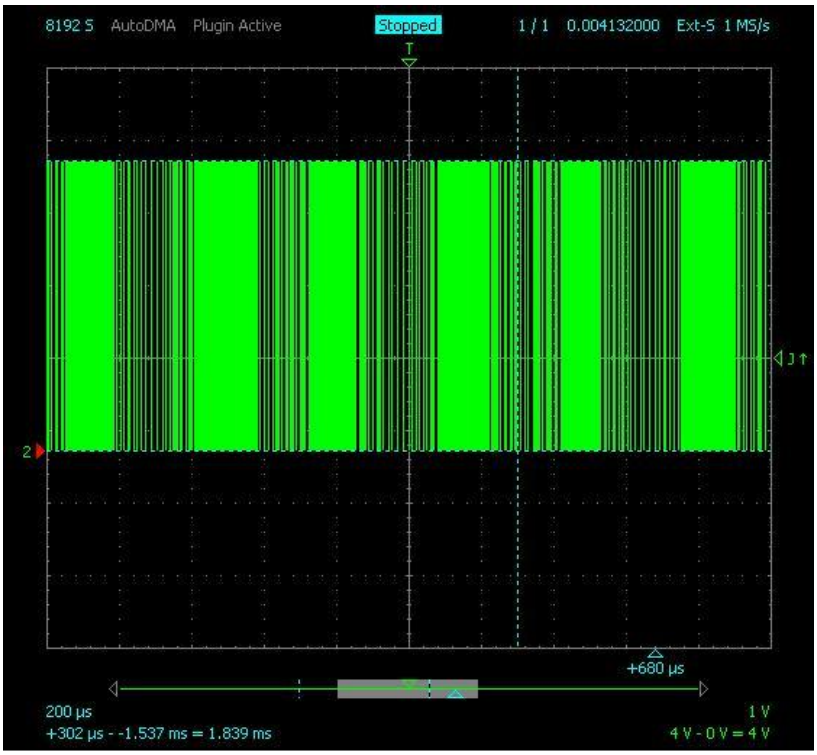

Figure 48. One-bit data stream output from the sigma-delta modulator using the AD712

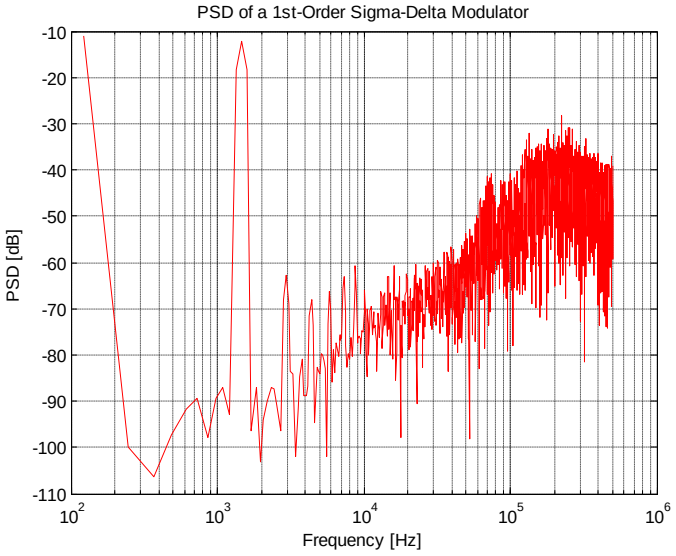

Figure 49. PSD plot of the sigma-delta modulator using the OP AMP AD712.

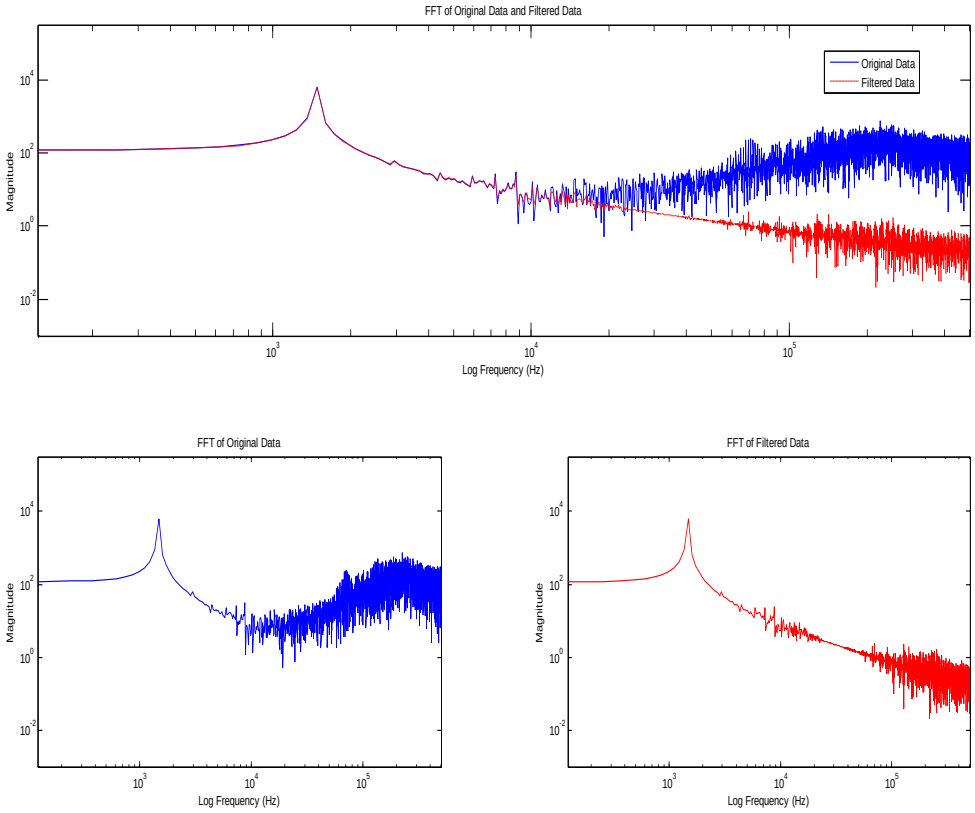

Figure 50. FFT comparison between unfiltered data (output of the modulator) in blue and filtered data (output of the A/D converter or FIR LPF).

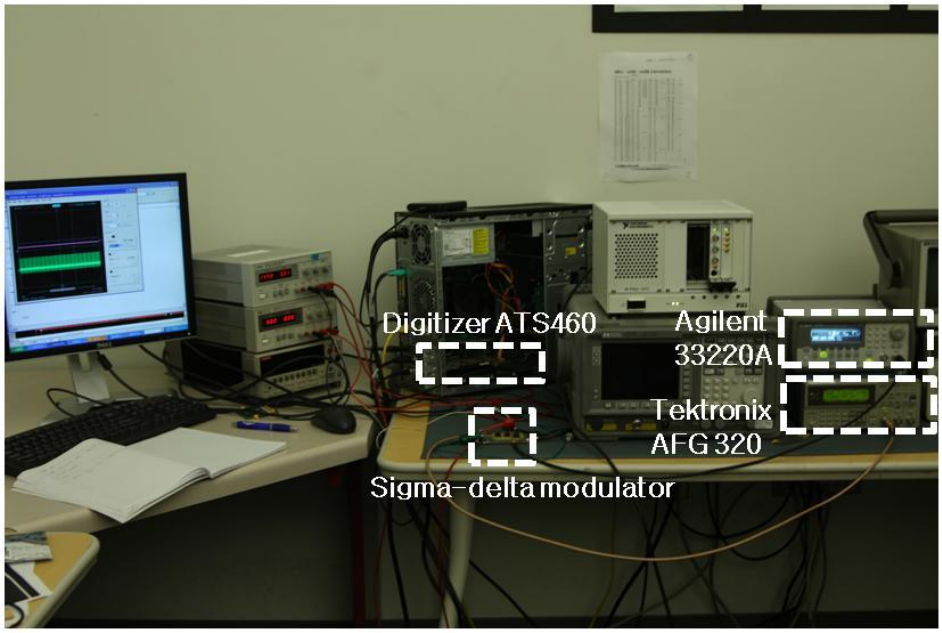

Figure 51. Measurement setup.

2.4.2 Experimental Results

The conventional dynamic test has been performed on the sigma-delta A/D converters with 60 operational amplifiers as shown in Table 4 by using a 14-bit single-tone sinusoidal signal with the input frequency of 1.4648k Hz and the amplitude of 5 peak-to-peak voltage and an offset voltage of 2.5V generated from Agilent 33220A arbitrary waveform generator (14-bit resolution, -70dBc harmonic distortion, THD of 0.04%, and phase noise of -115dBc). Then, the dynamic specifications such as SNR, THD, and ENOB have been measured from the spectrum analysis of the converters output.

In the proposed methodology, an optimized two-tone signal with frequencies of 0.5kHz and 1.43kHz and amplitudes of 3V and 1.2V has been generated using Agilent

33120A arbitrary waveform generator (12-bit resolution, -70dBc harmonic distortion, THD of 0.04%, and phase noise of less than -55dBc). Since the Agilent 33120A is one channel AWG, the two-tone signal has been generated with additional random noise to degrade the input signal in Matlab and downloaded into the Agilent 33120A via USB connection. The two-tone signal stimulus was applied to the all 60 devices. Then, 40 devices out of total 60 devices have been selected in a random manner as a training set, and the dynamic specifications of the other 20 DUTs have been estimated using the proposed methodology. The estimations of the dynamic specifications for the 20 sigma-delta A/D converters using the proposed methodology were compared to the actual measurements using the conventional FFT test in Figure 52, Figure 53, and Figure 54. This result is summarized in Table 5. The estimations of the proposed methodology are close to the actual specification values, and this result validates the proposed test. The estimations can be further enhanced if the number of training devices is increased.

Table 5. Specifications prediction RMS errors

Specification	RMS error
ENOB	0.2647
THD	1.5566
SNR	1.5740

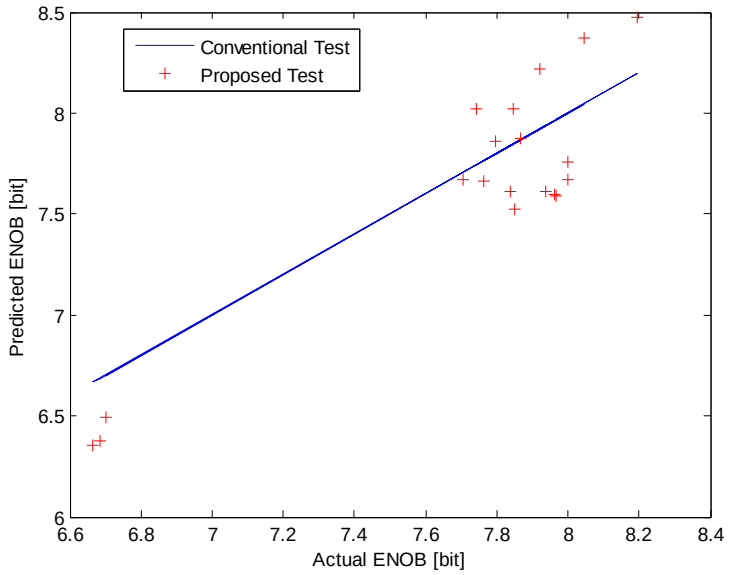

Figure 52. ENOB measurement using conventional test (blue) and using proposed test (red)

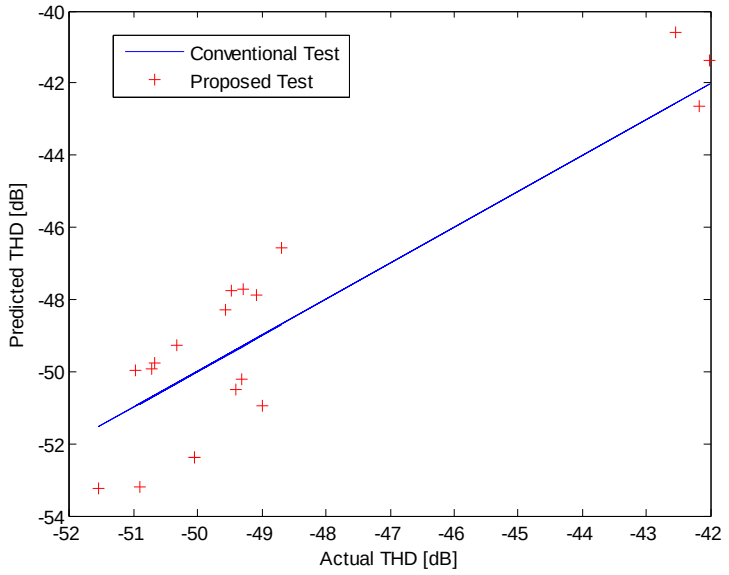

Figure 53. THD measurement using conventional test (blue) and using proposed test (red).

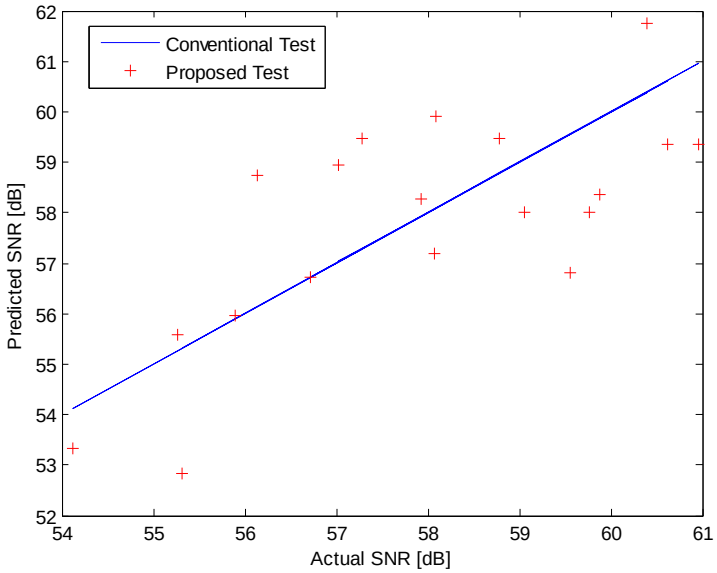

Figure 54. SNR measurement using conventional test (blue) and using proposed test (red).

2.5. SUMMARY

The proposed alternate-based test methodology for the high-resolution A/D converters specifications was presented in Chapter 2. With the proposed methodology, expensive spectrally pure signal generator and measurement equipment are not required. The methodology was validated in the simulation and hardware experiment. The test time can be reduced as compared to the conventional FFT test by predicting all the specifications at one time with one set of measurement. Limitations of the proposed methodology can be (1) the methodology needs to build a training set for a supervised learner, (2) the accuracy of the estimation highly depends on the volume of devices in the training set, and (3) the

conventional test must be performed using the high-cost test equipment for the training set. However, this proposed methodology is definitely an attractive approach that can reduce the test time and test cost once the training set is obtained, and the dynamic specifications of the high-resolution sigma-delta A/D converters can be precisely estimated.

CHAPTER Ⅲ

SIGNATURE-BASED DYNAMIC TESTING OF HIGH-RESOLUTION SIGMA-DELTA A/D CONVERTERS

The previous Chapter 2 presents the dynamic test solution for the high-resolution sigma-delta analog-to-digital converters (A/D converters) based on the *alternate test* approach. As discussed in the Chapter 2, the generation of a spectrally pure test stimulus and a clean clock signal are extremely challenging and costly for testing of the high-resolution A/D converters that have high-SNR and high-THD performances, and the proposed methodology presented in Chapter 2 allows the use of low-cost test instrumentation. However, the proposed alternate-based test technique requires a learning process with a set of training devices. To build a supervised learner with the set of training devices, the use of expensive high-precision test equipment are still required since the training devices must be pre-tested with the high-precision test input using the conventional test methodology. As an example in the hardware experiment of Chapter 2.4, 40 devices have been pre-tested using the conventional test to build the supervised learner. To increase the accuracy, more than 40 devices might be needed. As the volume of the training devices increases, the estimation accuracy of the specifications can accordingly increase. In addition, when a test setup or measurement setup is changed, a new set of training devices must be required for testing the devices in the new test environment. To overcome such drawbacks, another testing solution for the dynamic testing of the high-precision sigma-delta A/D converters is proposed in Chapter 3.

The Chapter 3 presents a *signature-based test and diagnosis methodology* for the dynamic specifications of the high-precision sigma-delta A/D converters using a multi-tone test input signal. In the proposed test methodology, the response of a behavioral model of the A/D converters incorporating its key module level non-idealities is matched with the response of the A/D converters under test by solving a nonlinear optimization problem that finds the best non-ideality parameters corresponding to the observed DUT test response. The dynamic specifications of the A/D converters are then calculated from the derived model parameters. This proposed signature-based test methodology in Chapter 3 has many aspects in common with the alternate-based test presented in Chapter 2 as follows: (1) The multi-tone test stimulus is designed in such a way as to maximize the accuracy with which the model non-ideality parameters can be calculated from the observed test response using the genetic test stimulus optimization algorithm, and (2) the digital pulse sequence at the output of the sigma-delta modulator is made externally observable and utilized as a test access point for the test response analysis. A key contribution is that the dynamic specifications such as ENOB, SNR, and THD of the converter and the module level non-idealities contributing to those specifications can be simultaneously determined from the derived model parameters. The test method is fast, and diagnosis is accurate. The goals and objectives of the proposed methodology are summarized as follows:

1. The proposed methodology develops a low-cost test methodology for the dynamic specs (ENOB, THD, SNR) of the high-precision sigma-delta A/D converters. The low-cost test can be achieved by using the optimized multi-tone test signal, which is a lower resolution signal than the resolution of the A/D converters under test. The

latter requires increasing the sensitivity of the test response measurements to behavioral perturbations of the A/D converter to the maximum extent possible using test stimulus generation.

2. The proposed methodology develops an algorithm for estimating the DUT dynamic specifications from the observed DUT response using the model parameter estimation in such a way that the key A/D converters dynamic specification values (effects) and all the DUT module non-ideality parameters (causes of specification deviation) are *simultaneously* obtained from the analysis. This allows the cause and the effect to be determined on a per-chip basis from manufacturing test data and also eliminates the need for using the supervised learning algorithms for test data analysis, which is required in the proposed methodology in Chapter 2. Note that the use of model parameter estimation requires the development of accurate behavioral models of DUT non-idealities. This is accomplished with help from A/D converter designers.

The Chapter 3 is organized as follows: Since the issues for dynamic testing of the high-precision sigma-delta A/D converters are discussed in Chapter 2, it will be skipped in Chapter 3. Section 3.1 discusses a brief description of the prior signature-based test works proposed by other researchers. The proposed low-cost test approach is illustrated in Section 3.2. Then, the validations of the proposed methodology are provided using software simulation in Section 3.3 and hardware measurement in Section 3.4.

2.1. PREVIOUS WORK

The Chapter 2.1 introduces the prior testing methodologies for the dynamic specifications of the high-precision A/D converters, and Chapter 3.1 discusses only signature-based test methodologies for the data converters proposed by the past researchers. The signature-based testing is a methodology that predicts or measures the specifications of the devices under test (DUTs) from the DUTs output or response, called the signature, with the response of the golden devices. The following will introduce the prior signature-based methodologies from the past, which use the signatures or responses of the DUTs for testing.

The authors in [48] use a software-generated digital stimulus to test a second-order sigma-delta modulator. In this methodology, the nonlinearity of the software-generated test input is known, and once the signature or the response of the DUT is captured, the DUT signature is adjusted using nonlinearity information of the stimulus to predict the SNRs. In [57], the authors propose to predict the specifications of a 12-bit pipelined A/D converters using a signature result out-of-range percentage (ORP) method. In the proposed method, the authors apply a cost-effective, a low-quality, pulse wave as a test stimulus and predict the SNR. The accuracy of the precision must be improved. The authors in [58] build the error signature by comparing between the responses of un-calibrated A/D converters and the digitally-calibrated A/D converters. However, this method determines a pass/fail and does not reveal the specifications information. In [59], the proposed methodology constructs a correlation between the signatures of the golden device and the DUT and determines the pass or fail of the DUT. Then, the authors use the conventional test method

to test the only fault-free devices, so the test time and cost can be reduced compared to testing all the devices using the conventional method. The method still uses the conventional test.

However, above techniques do not provide the diagnosis information of the faulty DUTs and/or require performing the conventional test, while the proposed methodology in this Chapter 3 allows the testing and diagnosis of the high-precision sigma-delta A/D converters. Techniques in [29]-[33] provide the fault diagnosis for the A/D converters. These fault diagnosis techniques must be carefully designed for the specific architecture of A/D converters.

2.2. PPROPOSED METHODOLOGY

Chapter 3.2 presents the details of the proposed signature-based testing for the high-precision sigma-delta A/D converters. The proposed methodology is a low-cost model-parameter-estimation-based test and diagnosis methodology for the dynamic specifications of the high-precision sigma-delta A/D converters using a multi-tone test input generated by the genetic algorithm, which is introduced in Chapter 2. In the proposed test methodology, a nonlinear optimization technique finds the best set of non-ideality parameters of the behavioral model of the sigma-delta A/D converter that matches the response of the behavioral model with the response of the DUT. In other words, the nonlinear optimization solver is varying the nonlinearity parameters of the behavioral model until the response of the behavioral model agrees with the response (or signature) of the DUTs. The dynamic

specifications of the A/D converters are then extracted from the derived model parameters. The multi-tone test stimulus is optimized using the genetic algorithm in such a way as to maximize the accuracy with which the model non-ideality parameters can be accurately calculated from the observed test response. This optimized test stimulus is generated using the same genetic algorithm discussed in Chapter 2, and a two-tone signal is again chosen as the test stimulus in this proposed methodology since the usefulness of the two-tone signal is observed in Chapter 2. For test response analysis, the digital pulse sequence at the output of the sigma-delta modulator is used as a test response. Therefore, the identical test scheme shown in Figure 17 is adopted in this proposed methodology. A key contribution is that the dynamic specifications such as ENOB, SNR, and THD of the converter and also module level non-idealities contributing to those specifications can be simultaneously determined from the derived model parameters.

The proposed methodology has many commons with the method described in Chapter 2 such as the use of sigma-delta modulator output and the test generation using the genetic algorithm. In comparison to the proposed methodology in the previous Chapter 2, the methodology in Chapter 3 eliminates *the use of the supervised learner* and provides additional *diagnostic information* in case the specifications of the DUTs do not meet the qualification levels. As a result, this proposed signature-based test methodology does not need to apply the conventional test method with the high-precision and expensive test equipment. In the following, the detail of the proposed test methodology is further described.

3.2.1 Overview of Test Setup

The configuration of the proposed signature-based test and diagnosis approach is depicted in Figure 55. The proposed methodology has two key steps as summarized:

Step 1, Test Stimulus Optimization: First, the phase and magnitude of each tone in the multi-tone stimulus is optimized. This procedure is identical to the one in Chapter 2, and it is seen that the use of two tones gives near-optimal results in Chapter 2. As shown in Figure 55, a set of "bad" DUTs (or faulty DUTs) are created in the software simulation to represent a diversity of DUTs non-idealities, and the *same* test stimulus is passed through the "bad" DUTs and the corresponding behavioral model of the DUTs. For each "bad" DUT, the behavioral model parameters (non-idealities) are determined using a nonlinear solver to see how accurately the DUT can be diagnosed (i.e. its specifications and non-idealities computed). This diagnosis capability across the sample of "bad" DUTs chosen is captured in an appropriately formulated cost function that is optimized by the genetic optimizer to give the optimized test stimulus. Note that this procedure indirectly maximizes the sensitivity of the test response to DUT behavior perturbations in an indirect manner. This procedure is depicted in the lower loop of Figure 55.

Step 2, Manufacturing Test and Diagnosis: During the manufacturing test and diagnosis, the optimized test stimulus is directly applied to the DUT (hardware) in question and the behavioral model of the DUT. The model parameter estimation using the nonlinear solver is directly performed using the observed DUT response as a reference, and all the DUT

behavioral model non-ideality parameters and all its dynamic specifications are computed simultaneously from the test response data. This is shown in the upper loop of Figure 55.

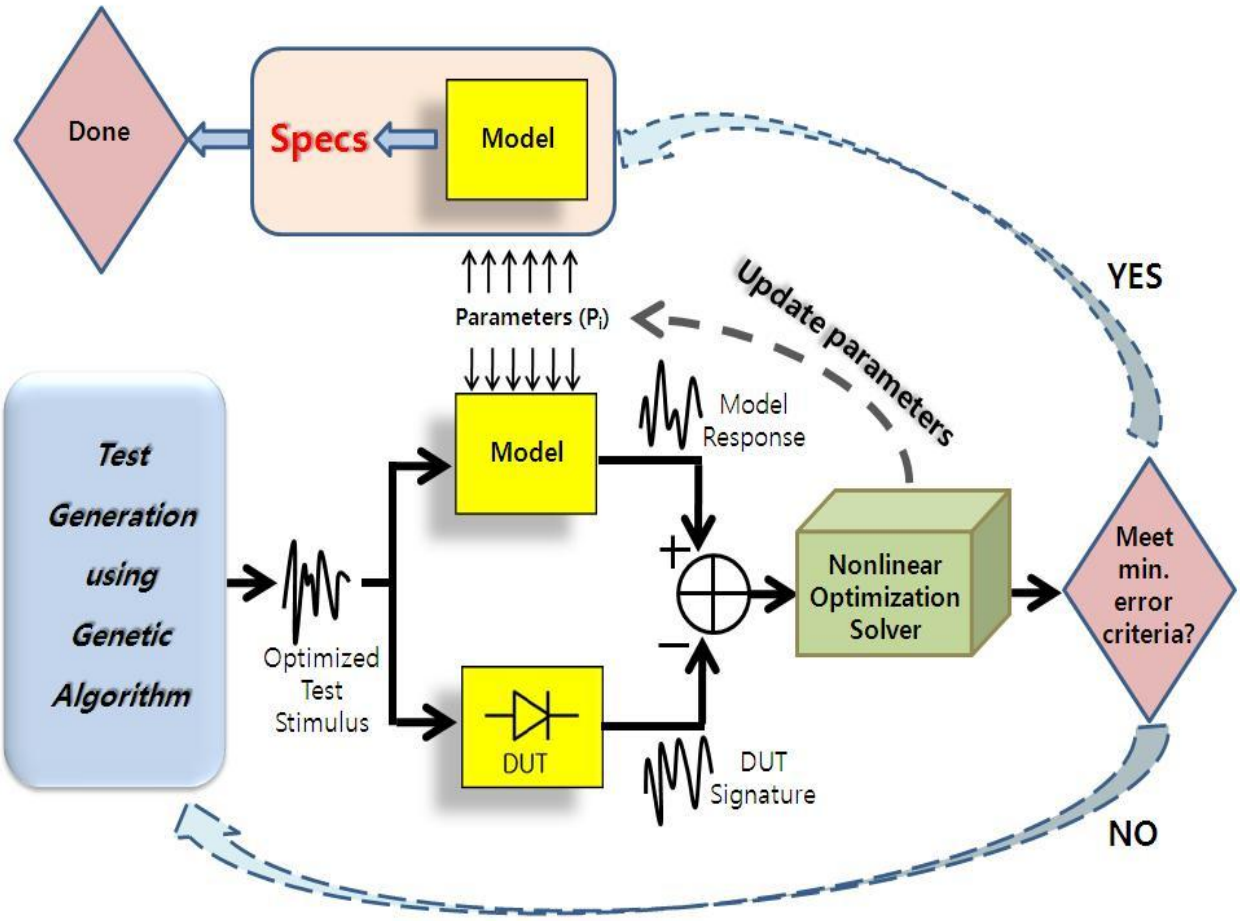

Figure 55. Proposed test approach configuration.

3.2.2 Test Generation using Genetic Algorithm

The test generation algorithm is identical to the one used for the alternate-based test approach in Chapter 2, but a new optimized test stimulus must be regenerated with a new cost function because the main approach of specifications prediction in this methodology differs from the methodology in Chapter 2. It is seen in Chapter 2 that the optimized two-tone stimulus, generated by the genetic algorithm, gives near-optimal test performance at a fast time, and hence the two-tone stimulus is chosen as the stimulus of choice in this proposed methodology. A multi-tone stimulus with more than two tones might outperform the performance of the two-tone stimulus, but the genetic algorithm consequently takes longer time to converge and find all the parameters for the multi tones than finding the parameters of the two tones. In testing, an ideal case is to find a relatively good or acceptable test generation solution at a relatively fast time, so the test time can be reduced. The phase and magnitude of each tone must be optimized for the maximum test and diagnosis accuracy. The amplitude and frequency of this two-tone input stimulus is optimized in such a way that the error in model parameter computation is minimized. A nonlinear solver is used to determine the behavioral model parameters from the observed response to each candidate test stimulus across the population of DUTs considered. The squared error between the computed and known DUT model parameters summed over all the DUTs is used as a cost function for the test stimulus optimization. In the genetic algorithm, the optimal values of the two-tone stimulus can be found after iterations when the squared error of the cost function is minimized.

3.2.3 Test Response Observation

Due to their noise shaping property that pushes noise power to the out-of-band, the sigma-delta A/D converters can achieve relatively high-resolution with high-SNR as compared to the other architectures of A/D converters. However, Chapter 2 examines that the out-of-band component, which is removed by the digital filter, contains valuable information about the sigma-delta A/D converters nonlinearities. To prevent such useful nonlinearities information in the "out-of-band" spectrum from being masked by the digital filter, the proposed methodology in Chapter 3 adopts the same DfT methodology as presented in Chapter 2. The simple block-diagram introduced in Chapter 2 is seen in Figure 17 and also used in this test scheme. For determining the non-ideality parameters of the behavioral model of the DUT, the frequency spectrum of the digital bit-stream at the sigma-delta modulator output (hardware output) is captured, and the model parameters are computed using the nonlinear solver to match the simulated frequency spectrum with the observed frequency spectrum of the actual DUT. The spectrum considered is that of the digital bit stream of the modulator output prior to digital filtering and is referred to as the "full-band" spectrum, which is more strongly correlated with the specifications of the DUT than the "in-band" spectrum obtained after digital filtering and hence increase test response sensitivity. The sensitivity of the components in the full-band (in-band component + output-of-band component) is increased with the optimized test input, and thus this property allows the nonlinear optimization solver to find the parameter values that match the behavioral model response to the DUT output much faster and easier than observing

only in-band components. Therefore, the modulator bit-stream output is used as the response of the model and the signature of the A/D converter under test.

3.2.4 Determining DUT Model Parameters

This Section 3.2.4 discusses the technique to determine the model parameters (DUT nonlinearities) from the analysis of DUT response and behavioral model output. The problem of determining the DUT model parameters is reduced to an optimization problem:

Optimization Problem: Find the "best" model parameter values that cause the response of the DUT model to the applied test to match the observed DUT response to the maximum extent possible.

To minimize the error between the two responses of the model and A/D converter under test corresponding to the optimized two-tone test stimulus, numerous candidate optimization techniques are available, and the proposed methodology uses one of nonlinear solvers available in Matlab optimization toolbox. The nonlinear solver is based on Nelder-Mead simplex direct search methodology.

In the multi-variable optimization, it is not easy to visualize the impact of multi-variable changes. Nelder-Mead simplex direct search method extrapolates the behavior of the objective function measured at each test point arranged a simplex and finds a new test

position. If the point is better than the best current point, the method stretches exponentially. Otherwise, the method shrinks the simplex to a better point. This search algorithm is fairly simple and fast yet effective enough in the proposed approach. In addition, the optimization toolbox provided from Mathworks is easy to use. In next Chapter 3.3, the simulation results using the above concept are provided.

2.3. SIMULATION RESULTS FOR VALIDATION

The proposed methodology was validated in the computer simulations. In Matlab and Simulink, 300 instances of a 16-bit sigma-delta A/D converter were implemented with small and large process variations, each instance with a unique combination of parameter (nonlinearities) values that must be estimated. To validate the test objective of using low-cost (low-resolution) test input, the test stimulus was modeled as a 14-bit precision signal with 80 dB SNR. The optimal two-tone stimulus (14-bit precision and 80 dB SNR) was generated using the genetic algorithm. Figure 56 shows the performance of the genetic algorithm reducing the fitness function at every generation. The algorithm converges to the best solution after 40 generations (Amp1=0.2367, Fin1=1.174kHz for 1^{st} tone and Ampl2=0.4586, Fin2=1.09kHz for 2^{nd} tone). In summary, the genetic algorithm improves the solution almost eight times better than initial solution and also improved the mean fitness value about 30 times. This result shows the effectiveness of the genetic algorithm.

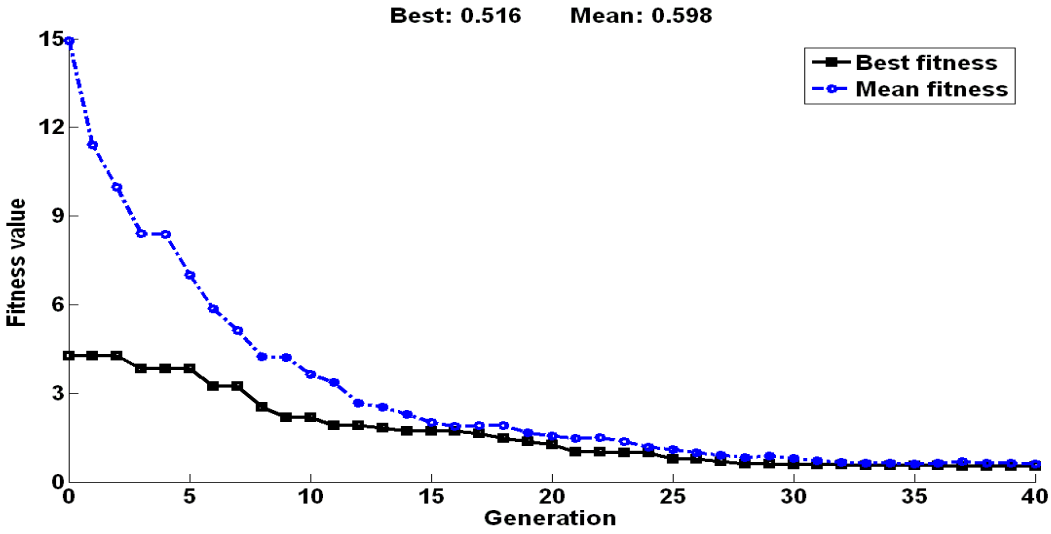

Figure 56. Genetic Algorithm Performance.

The optimized two-tone test stimulus was then applied to the 300 instances (DUTs) and the behavioral model. The parameter values of the model were initially set to one identical set of parameter values for the 300 instances. This pre-assigned parameter values were optimized by the nonlinear solver until the model responses were agreed with the captured responses of the 300 instances. Simultaneously, the dynamic specifications for the 300 devices were calculated with the estimated parameters.

Figure 57 presents the model parameters (nonlinearities) estimations for the 300 instances. Further, in Figure 58, the corresponding specification calculations for the 300 DUTs using the proposed signature-based test approach (red +) are compared to the conventional FFT test (blue **x**) and the alternate-based test (black •) proposed in Chapter 2. Each graph shows the measured values on the y-axis and the actual values on the x-axis.

It is seen in Figure 57 that majority of model nonlinearities can be accurately estimated except input bias and PSRR. However, the device specification values (ENOB, SNR and THD) for the 300 instances corresponding to the estimated parameters can be measured precisely as seen in Figure 58. One possible reason might be because the input bias and PSRR parameters do not affect the dynamic specifications significantly and/or are masked by other dominant parameters. According to the simulation results, the proposed technique can accurately test the sigma-delta A/D converters specifications and provide diagnosis information (nonlinearities) despite bad estimations for the input bias and PSRR. Note that ENOB is obtained from signal-to-niose-and-distortion (SiNAD) and differs from SNR.

Figure 58 shows that the conventional FFT test (blue **x**) using the coarse input stimuli fails to measure DUTs with about 11-bit or higher resolutions, while the proposed technique in Chapter 3 (red +) and the technique in Chapter 2 (black •) can test all the instances with high-accuracy. In addition, significant improvements of the proposed signature-based test approach in Chapter 3 from the technique in the alternate-based test approach in Chapter 2 are (1) no need for the pre-training set for the supervised learner using the conventional test and (2) diagnosis capability for faulty devices. The alternate-based technique must apply the conventional FFT test with spectrally pure test stimulus to the reasonable number of devices for the supervised learner, which is not required in the signature-based approach. Once a test environment changes, a new set of training devices is needed. In addition, the proposed signature-based approach reveals what non-idealities cause the devices to become faulty, which is a new and powerful feature.

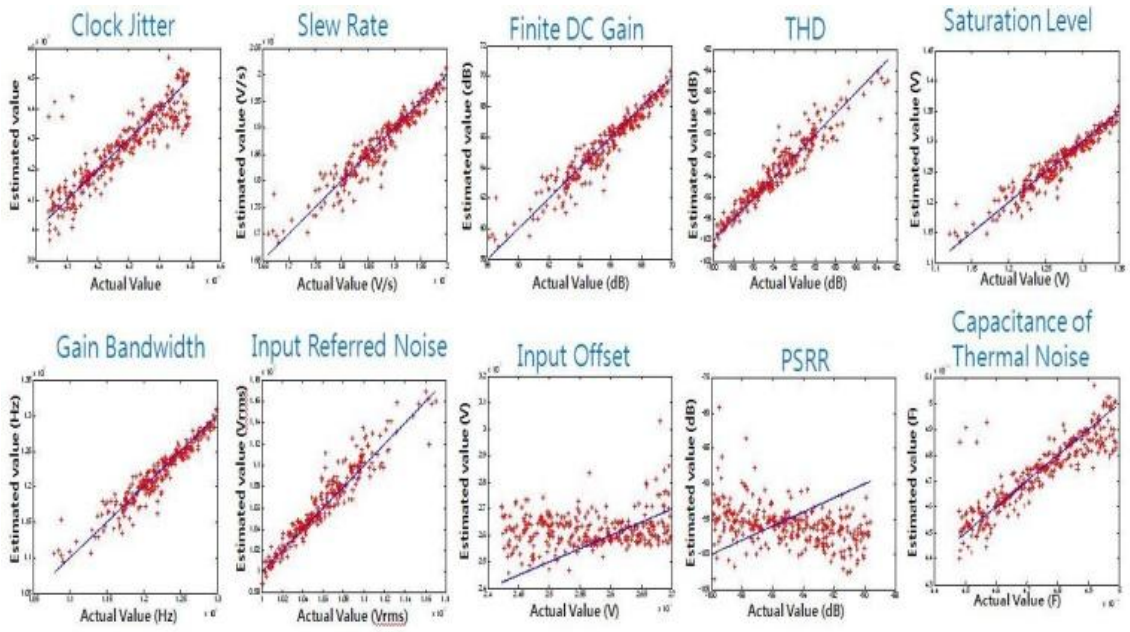

Figure 57. Model parameter estimations.

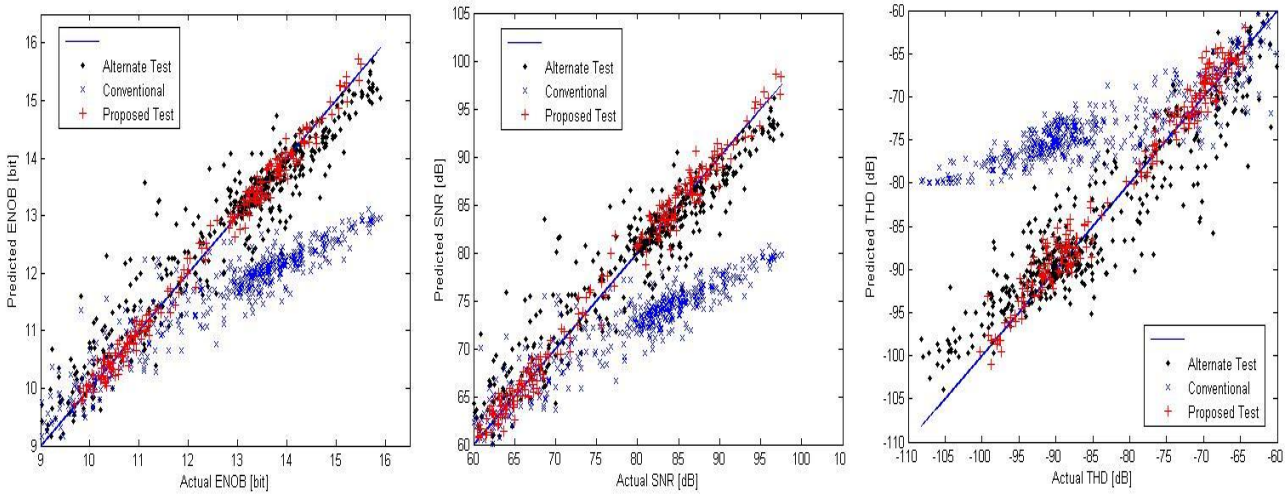

Figure 58. Proposed method predictions versus alternate-based method predictions (Chapter 2) versus conventional method measurements using 14-bit input stimulus

The overall comparison of the measurement errors for the three different test methodologies, which summarizes Figure 58, is given in Table 6. It is seen that the proposed signature-based approach gives the most accurate prediction results among the others. Similar to the alternate-based test approach in Chapter 2, this signature-based test technique enables testing the high-resolution sigma-delta A/D converters using lower resolution test input, which reduce the test time and test cost compared to the conventional FFT test methodology.

Table 6. Specifications measurement errors (RMS)

Specs.	Signature-based approach	Alternate-based approach	Conventional FFT
ENOB	0.1660	0.5374	1.0388
SNR	1.2746	3.2352	6.2538
THD	1.7397	4.3827	9.2719

2.4. VALIDATION OF PROPOSED METHODOLOGY

The hardware experiment was performed to validate the proposed signature-based test methodology for the high-resolution sigma-delta A/D converters, and Chapter 3.4 presents the hardware experiment. The proposed methodology estimates the specifications of the sigma-delta A/D converters and reveals the nonlinearity parameter values (operational

amplifier nonlinearity). Hence, the hardware experiment must include the measurement of the nonlinearity and the dynamic specifications of the sigma-delta A/D converters.

3.4.1 Operational Amplifier Measurement

In addition to the estimations of the sigma-delta A/D converter specifications, one of the key contributions of the proposed signature-based methodology is a diagnosis capability. Since a set of the behavioral model nonlinearities is optimized and characterized in such a way that the behavioral model performs the same as the DUT performs, the specifications of all 60 operational amplifiers presented in Table 4 must be measured for the validation of the diagnosis capability. The operational amplifiers were bread-boarded with all passive components (capacitors and resistors) and measured, and an example of the finite open-loop gain measurement for the operational amplifier LF353 on the breadboard is shown in Figure 59. The measurement procedures for other specifications of the operational amplifiers are briefly described in the following subsections.

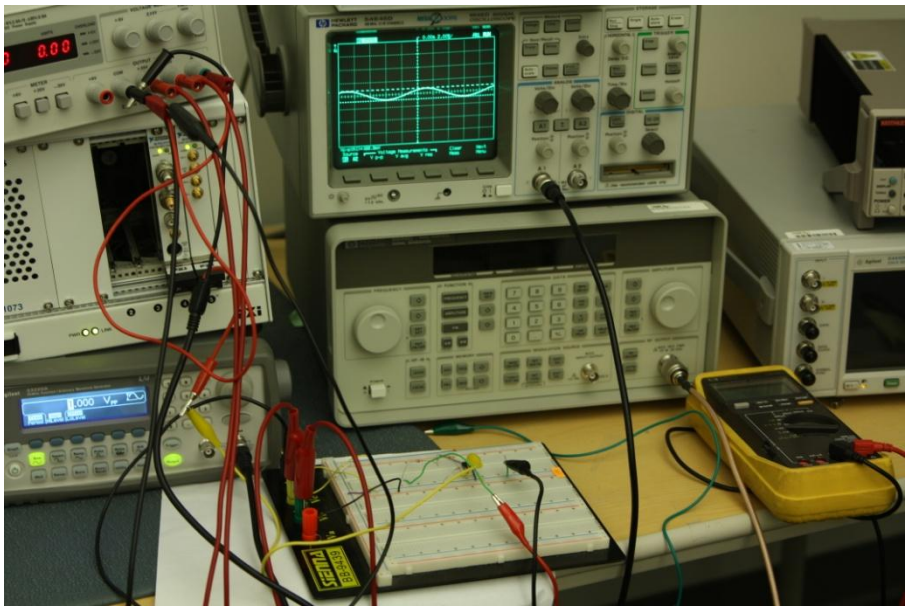

Figure 59. Open-loop gain measurement of an operational amplifier.

3.4.1.1 Open-Loop Gain Measurement

The open-loop gain of an ideal operational amplifier is infinity theoretically, but a real operational amplifier has a finite open-loop gain due to the nonlinearity effects. However, this finite open-loop gain is still large, commonly 100,000 to over one million, so a direct measurement at the output of the amplifier by applying an input signal is not possible since the output of the amplifier corresponding to the input signal value multiplied by the large open-loop gain will be clipped and saturated. Even with an extremely small input voltage value applied to the amplifiers, the measurement is still difficult without appropriate equipment. Even if the extremely small voltage is applied to the operational amplifier, a bias voltage with the small input voltage would be amplified together by the open-loop gain,

and an accurate measurement is not easy. Therefore, the finite open-loop gain was measured using a feedback loop, and Figure 60 presents a general test setup (schematic) for the measurement. With such negative closed-feedback loop, the bias voltage effect can be ignored, and the output voltage measurement becomes easy. The open-loop gain is then approximately 101 times a ratio of V_{out} to V_x : [(R7 + R8)/R8] x (V_{out}/V_x). More accurately, the values of the resistors R7 and R8 were measured as 986.2 ohms and 98.24k ohms, respectively, using a digital multi-meter (DMM) HP 974A from Hewlett Packard. The input signal and output of the amplifier were measured using the digitizer ATS460.

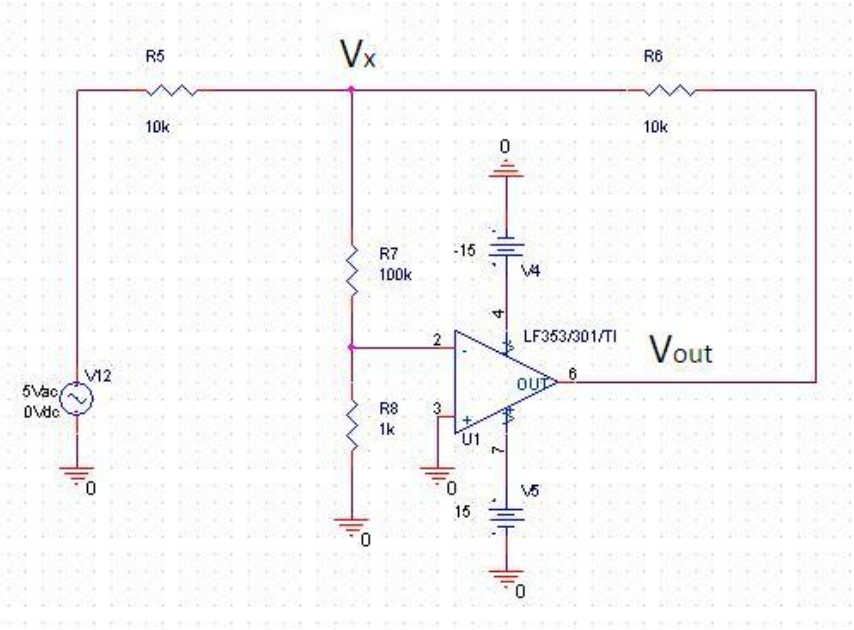

Figure 60. Schematic for finite open-loop gain and gain bandwidth measurements.

3.4.1.2 Gain-Bandwidth Measurement

The above open-loop gain must be measured over a range of frequency, and the open-loop gain starts to fall off at high-frequency as a result of its limited ability to quickly charge the node capacitances. A gain-bandwidth, also called unity-gain bandwidth, is the frequency of the input signal at which the gain drops to 0dB (or 1V/V). Therefore, the gain-bandwidth can be also measured using the identical test setup in Figure 60 by varying the frequency of the input signal. In the case of the ideal operational amplifier, the gain-bandwidth should be also infinite, but the gain-bandwidth is finite in reality, leading to the bandwidth limitation that causes a phase difference between the input signal and the amplifier output.

3.4.1.3 Input Offset Voltage Measurement

The ideal operational amplifier has a zero offset voltage (or current) because the ideal device has no leakage or bias current into the device. The real operational amplifier has a small offset voltage at the input terminals of the device. Figure 61 describes a schematic to measure the input offset voltage. DC voltage is applied to the input of the operational amplifier, and the amplifier output is measured using a digital multi-meter (DMM) HP 974A from Hewlett Packard, which can measure from 500mV with a resolution of 10uV. The offset voltage, V_{off}, can be measured as $V_{off} = V_{out} - V_{in}$. This measurement was repeated with different values of the DC input voltage values, and then the offset voltage was averaged over all the measurements.

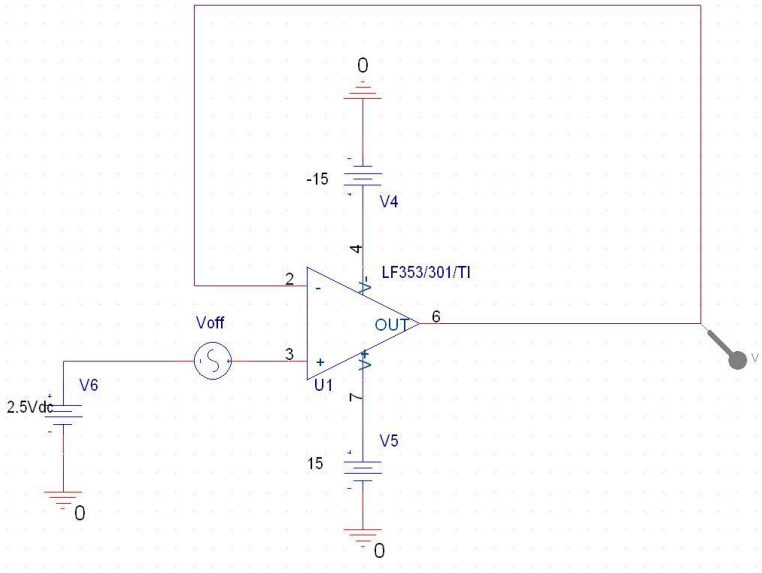

Figure 61. Schematic for input offset voltage measurement.

3.4.1.4 Output Voltage Swing Measurement

Output swing (or saturation level) of the operational amplifier must be measured since the output voltage is limited by the power supply rails. Figure 62 provides a measurement setup for the output swing. To measure the output voltage swing, a range of DC voltage value of V7 in Figure 62 is applied to the operational amplifier, and the corresponding output voltage value is measured using the digital multi-meter. Then, the saturation level is found at where the output voltage is clipped, which is a smaller value of the power supply rail-to-rail.

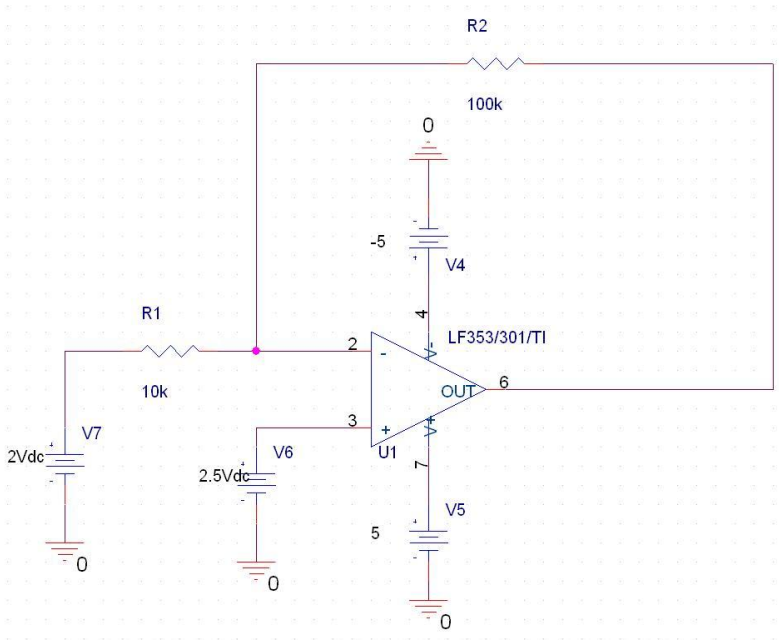

Figure 62. Schematic for output swing measurement.

3.4.1.5 PSRR Measurement

Then, power supply rejection ratio (PSRR) is measured using the test setup as shown in Figure 63. In an ideal case, the output of the operational amplifier does not change when the power supply voltage varies slightly. The PSRR is a measure of how well the output of the amplifier rejects the small changes in the power supply, and it is a function of frequency. As a result, the PSRR is measured over various input frequencies. In this test setup in Figure 63, an AC source is connected in series with the power supply to the positive input terminal of the amplifier, and the negative input terminal is connected to the output of the amplifier through a feedback making a closed loop. Then, the input of the AC source and

the output of the operational amplifier are measured using the digitizer ATS460 for each frequency value of the AC source. The PSRR is defined as PSRR = $20\log_{10}(V_{in}/V_{out})$ [dB].

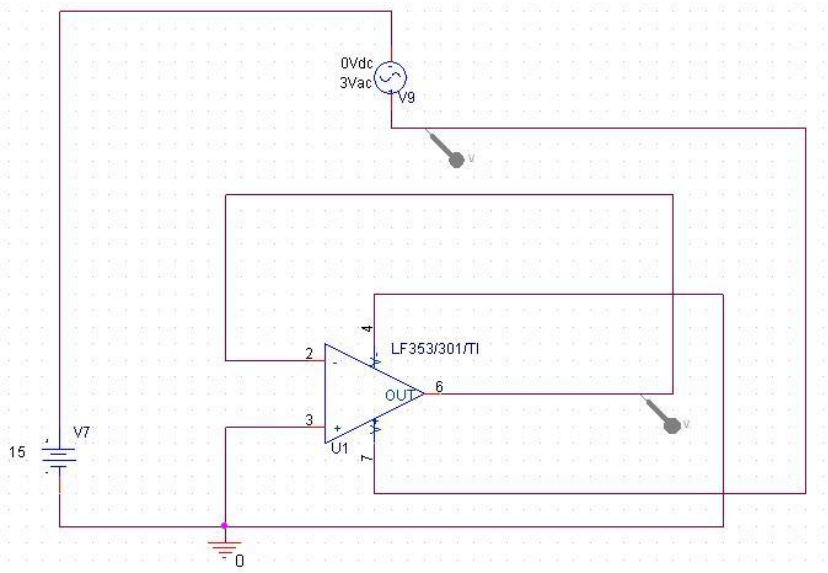

Figure 63. Schematic for PSRR measurement.

3.4.1.6 Slew Rate Measurement

Figure 64 describes the measurement setup for a slew rate of the operational amplifier. The slew rate is a maximum rate of a signal change, and the slew rate is caused by the insufficient current transfer to the output. Therefore, a pulse signal is generated using an arbitrary waveform generator and applied to the operational amplifier, and the corresponding output voltage and time were measured using the digitizer ATS460. The slew rate is measured by finding the slop of output voltage change, and hence the unit of the slew rate is voltage per a second.

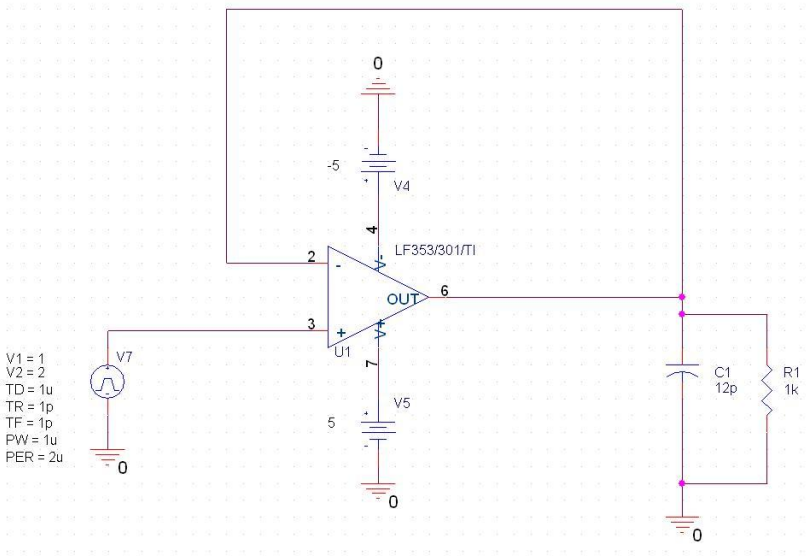

Figure 64. Schematic for slew rate measurement.

3.4.1.7 Total Harmonic Distortion (THD) Measurement

Total harmonic distortion (THD) can be measured using the measurement setup shown in Figure 64 by applying a sinusoidal input signal. The output of the operational amplifier was connected to the digitizer ATS460, and the THD was measured by calculating a ratio of the signal power to the sum of total 5^{th} harmonic distortions in dB.

3.4.2 Result of Hardware Experiment

This signature-based test methodology shares the identical design-for-test (DfT) scheme, and hence the sigma-delta modulator that is designed and used in Chapter 2 and the same

commercial devices (operational amplifiers, comparator, D-type flip-flop) will be used in this experiment. However, since signature-based methodology does not require a set of training set for the supervised learner, which was required in the alternate-based test methodology in Chapter 2, all the 60 DUTs can be tested in this experiment.

3.4.2.1 Hardware Experiment Setup

Again, a two-tone input signal with a first-tone frequency and amplitude of 476.2Hz and 1.5635V and a second-tone frequency and amplitude of 772.1Hz and 1.5635V respectively was generated from the Agilent 33120A arbitrary waveform generator, and a clock signal of 1MHz was generated using Tektronix AFG320. Then, the digitizer ATS460 acquired the outputs of the sigma-delta modulators and downloaded into a computer. Once all the responses of the sigma-delta modulators corresponding to the two-tone input signal were acquired and downloaded, the rest procedure was completed in the computer. The behavioral model of the 1^{st} order sigma-delta A/D converter incorporating its nonlinearities is presented in Figure 65. In this behavioral model, the response of the sigma-delta modulator model (before the digital filter) was taken to workspace in Matlab and compared with the downloaded response of the DUT (hardware). Then, the error between the response of the behavioral model and the response of the DUT was calculated. If the error did not meet the minimum requirement, a new set of nonlinearities for the behavioral model was generated from the optimization solver (Nelder-Mead simplex direct search algorithm) and fed to the behavioral model. This procedure was repeated until the error satisfied the

minimum requirement. When the error is less than the minimum requirement, this set of nonlinearities is used to produce the dynamic specifications (ENOB, THD, SNR). This test flow is described in Figure 66.

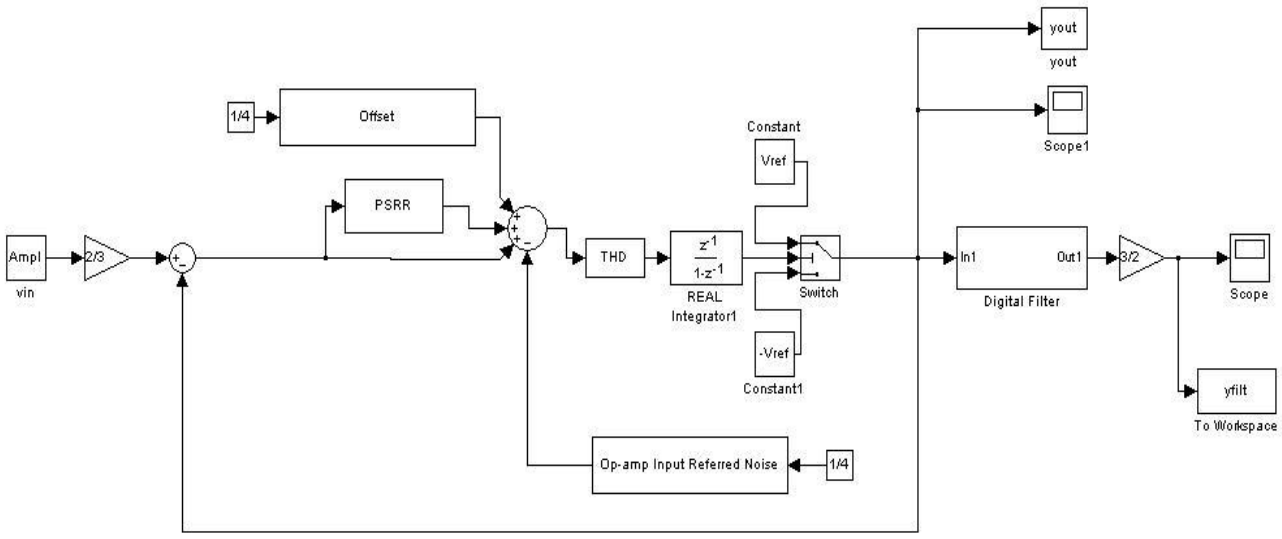

Figure 65. Behavioral model of 1st sigma-delta A/D converter

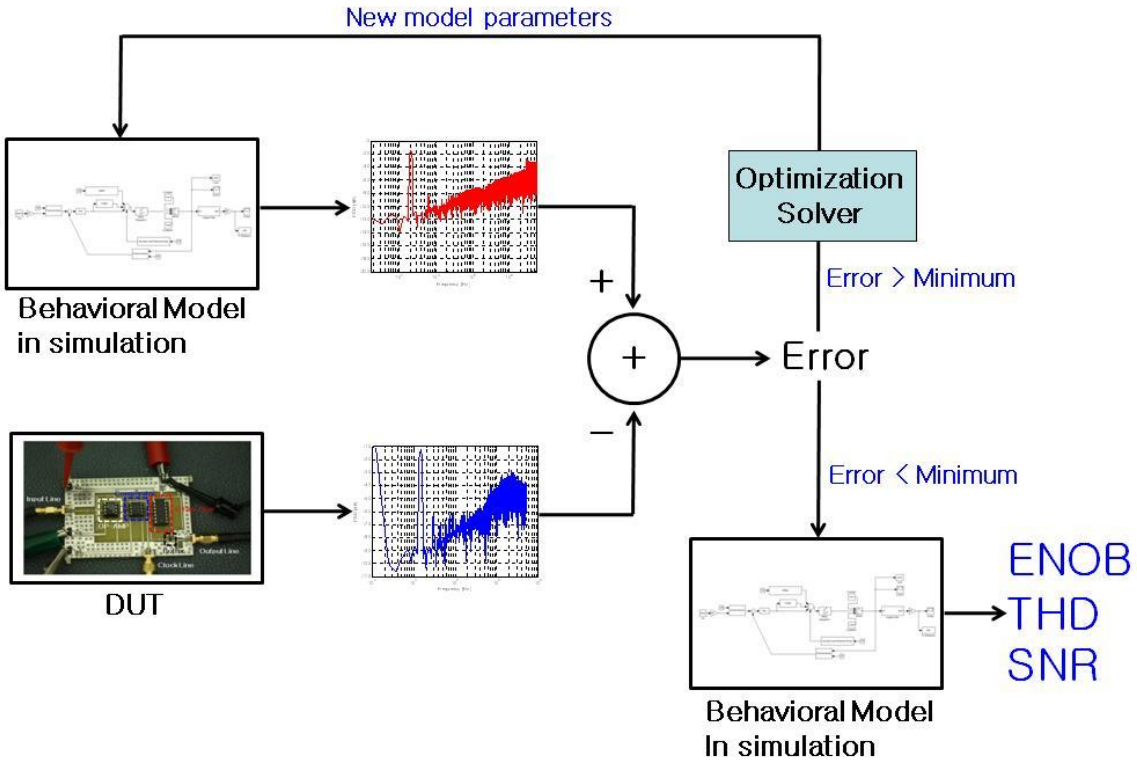

Figure 66. Test procedure

3.4.2.2 Experiment Results

The nonlinearities of the sigma-delta A/D converters (the specifications of the operational amplifiers) were determined from the optimization solver by matching the responses of the DUTs with the responses of the behavioral model. Then, the dynamic specifications for the sigma-delta A/D converters were estimated using the nonlinearity values. The estimation results are presented in this Section 3.4.2.2.

Figure 67, Figure 68, and Figure 69 present the estimation results of the dynamic specifications for the sigma-delta A/D converters using the proposed signature-based

methodology and compare the estimations with the measurements using the conventional FFT method. The actual specifications are shown on the x-axis, while the predicted specifications are shown on the y-axis. The dynamic specifications (ENOB, THD, and SNR) were accurately estimated for all 60 converters using the proposed methodology. The absolute maximum errors for ENOB, THD, and SNR were 0.0536-bit, 2.2246 dB, and 1.2876 dB, respectively. These errors between the estimation and measurements are relatively small considering the dynamic range of each specification.

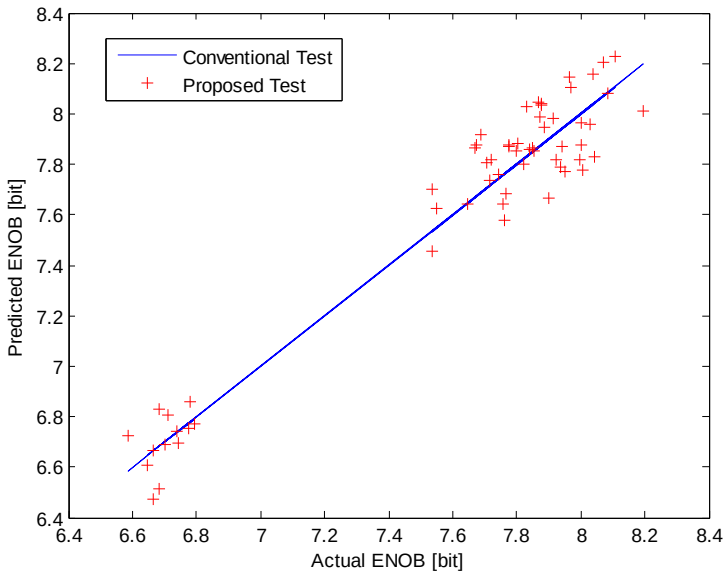

Figure 67. ENOB measurement using conventional test (blue) and using proposed test (red).

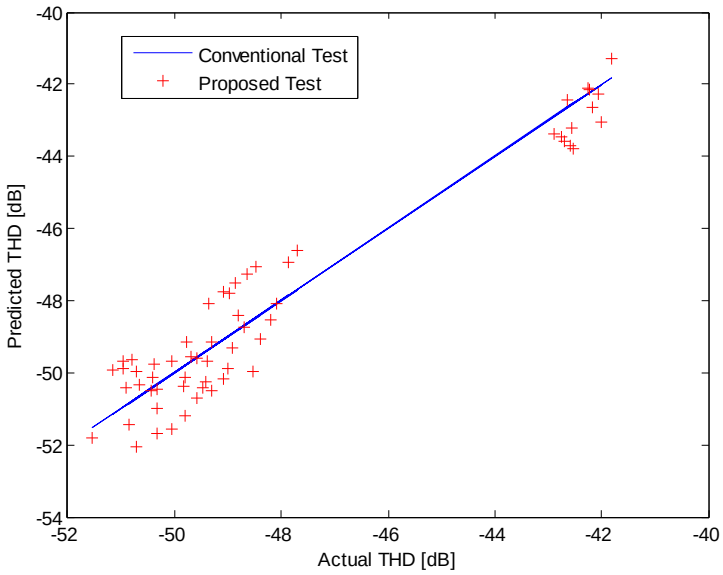

Figure 68. THD measurement using conventional test (blue) and using proposed test (red).

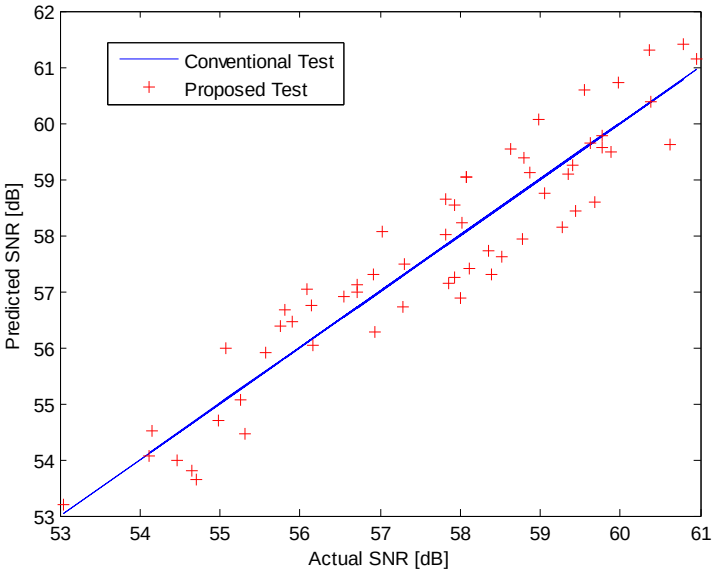

Figure 69. SNR measurement using conventional test (blue) and using proposed test (red).

Then, Figure 70, Figure 71, and Figure 72 compare the accuracy of the proposed results with the proposed alternate-based test in Chapter 2 and the conventional FFT test. In Figure 70 - Figure 72, the estimation results using the proposed methodology are presented with black •, while the estimation results using the alternate-based test and the measurements using the conventional FFT are shown with red + and blue line, respectively. For the comparison, only the dynamic specification estimations of the identical 20 devices using the proposed methodology were plotted in Figure 70 - Figure 72 because such 20 DUTs were estimated using the alternate-based test methodology and the other 40 devices were used as a training set. As seen in Figure 70 - Figure 72, the estimations using the proposed methodology were improved from the estimations using the alternate-based test. However, the estimation results of the alternate-based test can be also enhanced if a volume of the training set were larger. Table 7 summarizes the comparison results between the proposed signature-based methodology and the alternate-based methodology, and it is seen that the RMS errors for the 20 DUTs using the proposed methodology is about an half of the RMS errors using the alternate-based test. In addition, the proposed methodology does not require training devices for the supervised learner using the conventional test method. This aspect completely eliminates the use of high-precision and high-cost test equipment in the proposed methodology.

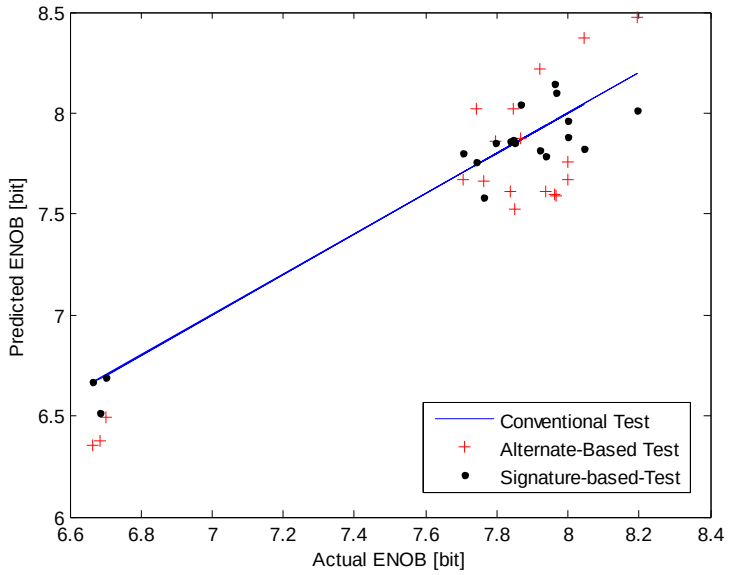

Figure 70. ENOB measurements using proposed method (black •) versus alternate-based method predictions in Chapter 2 (red +) versus conventional method measurements (blue).

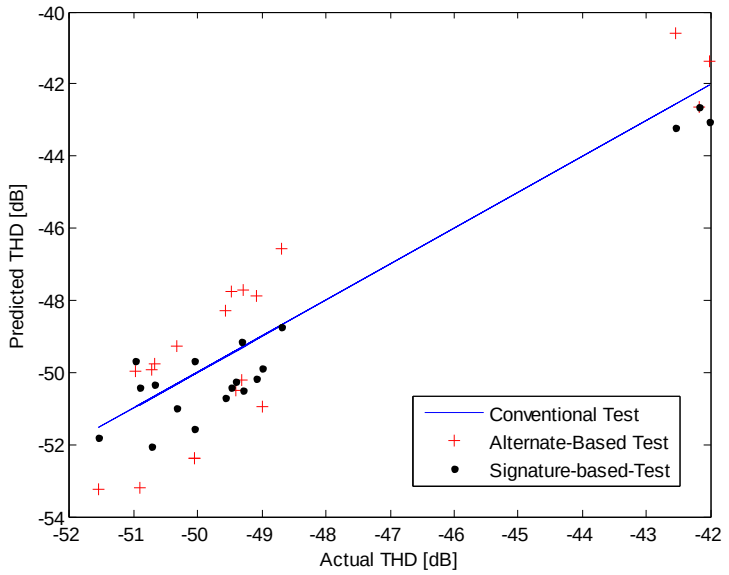

Figure 71. THD measurements using proposed method (black dot) versus alternate-based method predictions in Chapter 2 (red +) versus conventional method measurements.

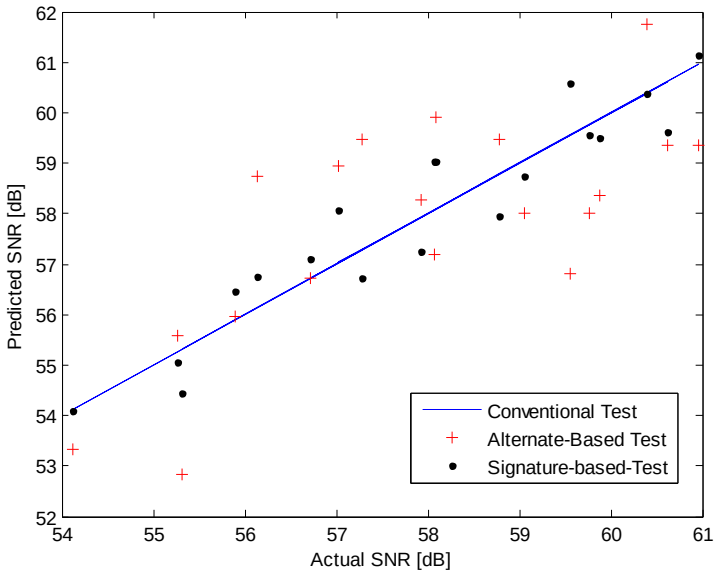

Figure 72. SNR measurements using proposed method (black dot) versus alternate-based method predictions in Chapter 2 (red +) versus conventional method measurements.

Table 7. Specifications measurement RMS errors.

Specifications	Proposed methodology	Alternate-based test
ENOB	0.1240	0.2647
SNR	0.8774	1.5566
THD	0.6684	1.5740

The parameter (nonlinearities of the converters) estimations that were found from the optimization nonlinear solver and let the behavioral model predict the dynamic specifications are presented in Figure 73 - Figure 79 and are compared to the measurement results in the experiment. All model parameters except PSRR were accurately estimated from the optimization nonlinear solver, and the bad estimations for PSRR were seen in the

simulation result of Chapter 3.3. While the estimations of input offset values were similarly bad in the simulation results, the estimations of the input offset values in this experiment were acceptably good. The most accurate parameter estimations were slew rate and gain-bandwidth. These slew rate and gain-bandwidth seem to be the most important specifications from the results.

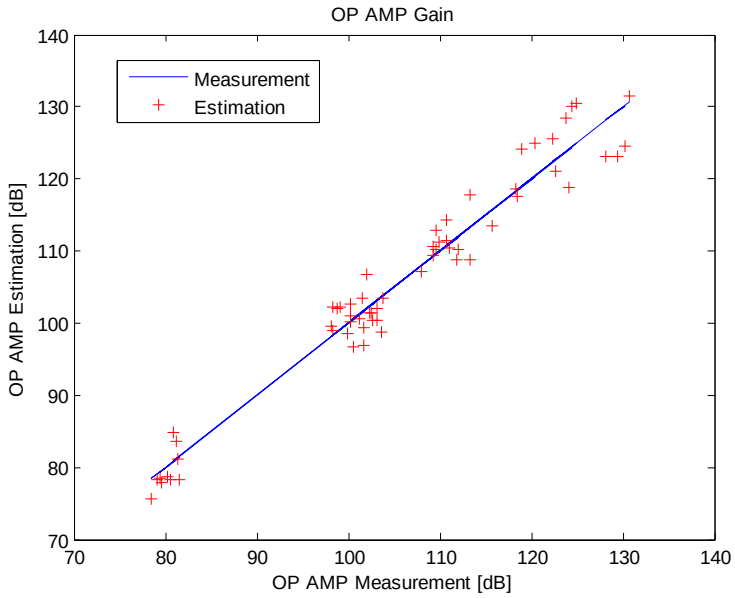

Figure 73. OP AMP open-loop gain measurement using conventional test (blue) and using proposed test (red).

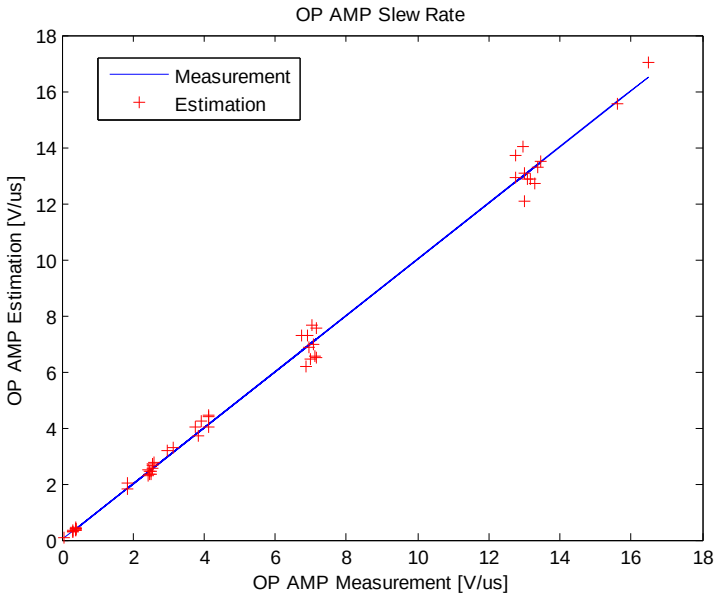

Figure 74. OP AMP slew rate measurement using conventional test (blue) and using proposed test (red).

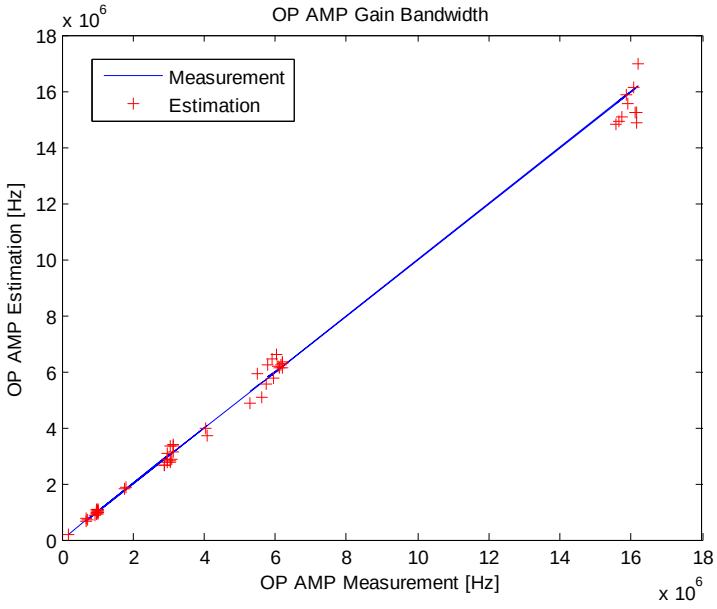

Figure 75. OP AMP gain-bandwidth measurement using conventional test (blue) and using proposed test (red).

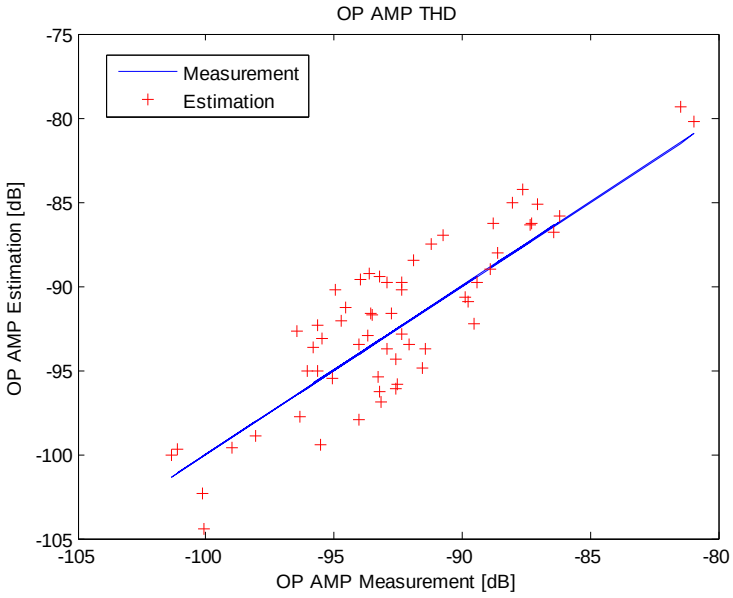

Figure 76. OP AMP THD measurement using conventional test (blue) and using proposed test (red).

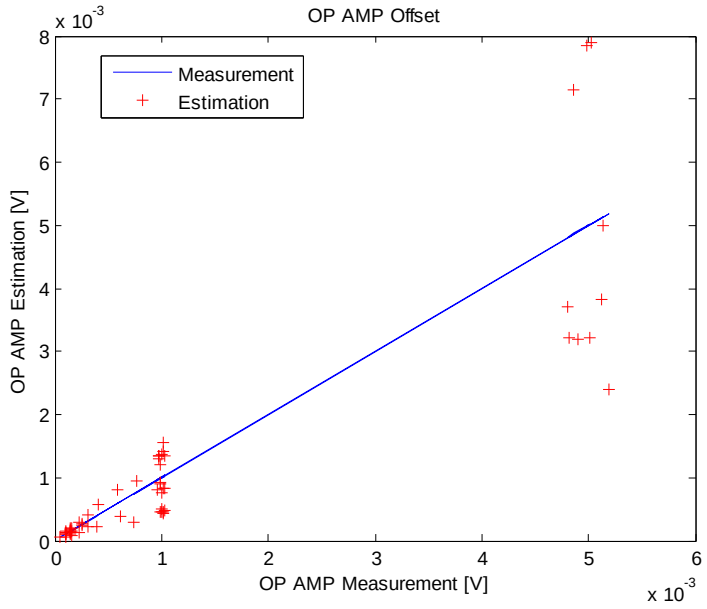

Figure 77. OP AMP input offset measurement using conventional test (blue) and using proposed test (red).

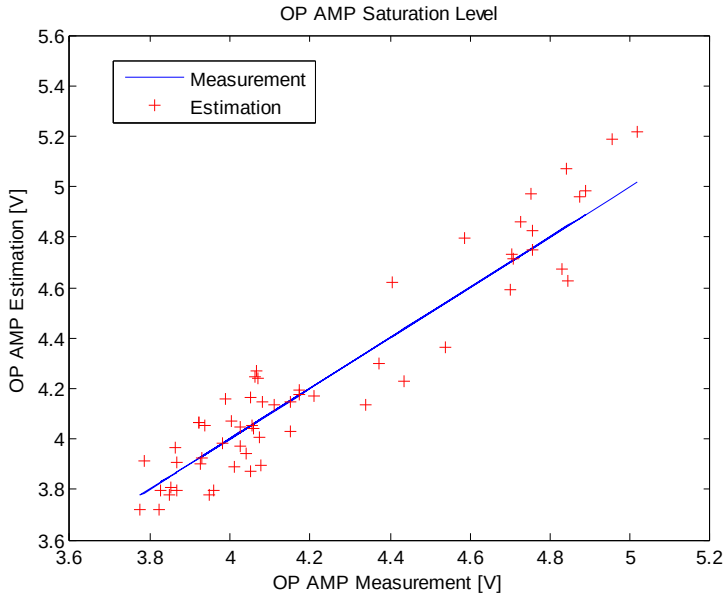

Figure 78. OP AMP saturation level measurement using conventional test (blue) and using proposed test (red).

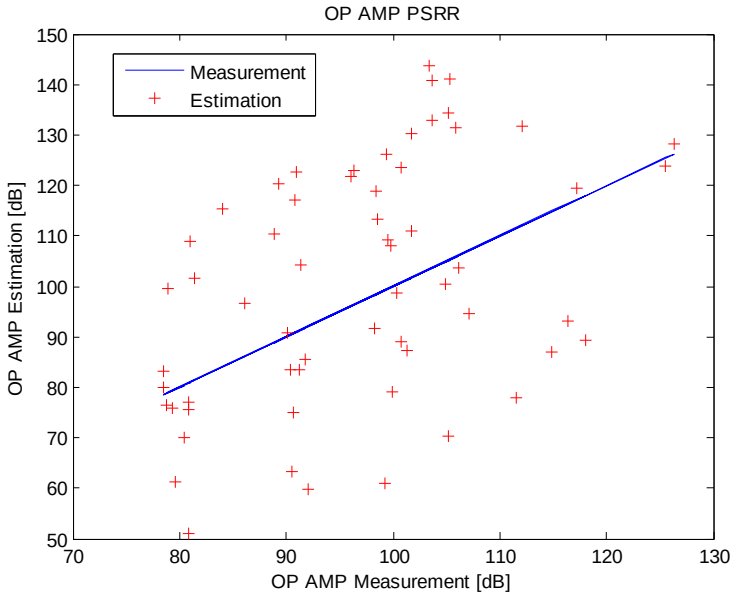

Figure 79. OP AMP PSRR measurement using conventional test (blue) and using proposed test (red).

2.5. SUMMARY

In Chapter 3, a low-cost dynamic testing and diagnosis methodology for the sigma-delta A/D converters was proposed. The proposed methodology is based on the model parameter estimation using a low-cost optimized test input. The nonlinear solver optimizes the parameter values of the sigma-delta A/D converters that simultaneously determine the dynamic specifications such as ENOB, THD, and SNR accurately. No expensive input stimulus generator is needed with the proposed methodology, which saves the overall test cost dramatically. The simulation results and hardware experiments validate the approach and show that the dynamic specifications and nonlinearities of the high-resolution sigma-delta A/D converters can be precisely measured with the imprecise optimized input stimulus. This proposed methodology overcomes the limitations of the proposed alternate-based test methodology in Chapter 2. In addition, the diagnosis capability is a powerful feature. However, the proposed methodology requires an accurate modeling technique that must be closely performing as the actual devices.

CHAPTER Ⅳ

STATIC SPECIFICATION TESTING OF HIGH-RESOLUTION A/D CONVERTERS

A low-cost methodology for linearity testing of high-precision analog-to-digital (A/D) converters using low-precision digital-to-analog (D/A) converters is proposed in Chapter 4. The proposed approach reduces both test time and test cost as a result of the measurement of fewer samples than a conventional histogram test method. The histogram-based test is a well-known standard method for the linearity testing of A/D converters as described in Chapter 1. However, this histogram methodology becomes infeasible as the resolutions of the A/D converters increase. In general, the average number of 30 to 40 samples per a digital code is collected with the histogram method. To guarantee the test quality, one or several hundred samples per a code might be required. A 24-bit resolution A/D converter consists of more than 16 million digital output codes (16,777,216 codes). When the 24-bit resolution A/D converter is tested using the histogram method by collecting the average number of 100 samples per a code, more than 1.6 billion samples need to be measured, which is impractical. Furthermore, the high-precision A/D converters have much lower sampling rates than high-speed and low-precision A/D converters in general, so collecting such a huge number of samples at a low-sampling rate indicates a long test time. As a result, the histogram test is not suitable for the high-precision A/D converter linearity test due to such a long test time. Test time is a big issue in production test, which significantly increases both the test cost and final production cost.

In addition to the long test time, the generation of pure analog input signals to the A/D converters under test is another issue. Past research work [4] indicates that the analog input signals that stimulate A/D converters under test must have at least 3-bit higher resolution and linearity than the A/D converters. This means that the analog input signals with minimum resolution of 27-bit must be needed for testing the 24-bit A/D converters. The generation of 27-bit or higher precision analog signal is extremely challenging and expensive. Such high-performance and expensive test-platforms lead to complex test solutions and significant contribution towards increasing the overall manufacturing cost of the products.

The proposed linearity test methodology uses lower precision analog input signals than the A/D converters under test with less measurement than the histogram test. The methodology does not require expensive test equipment and does not need to collect the huge number of output samples in contrast to the histogram test. The methodology estimates a transfer function of A/D converters under test using a polynomial-least-squares-fitting method by taking measurements at intermediate code points, and all the code widths are defined accurately. The main contributions of the proposed linearity test methodology can be summarized as follows:

1. The proposed methodology reduces the test time by measuring relatively smaller number of samples from the A/D converters under test than the conventional test.
2. The proposed methodology requires no expensive test equipment, while the conventional test requires expensive and high-precision test equipment.

3. The proposed methodology is robust to the nonlinearity present in the low-resolution D/A converters used in the test setup.
4. The cost of testing is dramatically reduced as a result of the reduced number of measurements and low-cost equipment compared to the conventional test.

In the rest of the Chapter 4, previous research works from other researchers related to the static linearity testing of the A/D converter are introduced in Chapter 4.1, and the proposed test methodology is illustrated in Chapter 4.2. Then, software simulation results are provided in Chapter 4.3, and the hardware experiment is presented in Chapter 4.4 to validate the proposed methodology.

4.1. PREVIOUS WORK

In Chapter 4.1, a brief summary of various research efforts involving the linearity test of the A/D converters is presented. Authors in [41], [60], and [61] propose built-in-self-test (BIST) schemes for integral non-linearity (INL) and differential non-linearity (DNL) test of the A/D converters. In [41], authors use a polynomial-fitting technique to map a transfer function of the A/D converters, but this method requires an on-chip A/D converter and D/A converter, which may not be feasible for many mixed-signal integrated circuits or systems. Authors in [60] propose another BIST scheme that does not require any on-chip A/D converter and D/A converter. Instead, the authors use the sigma-delta modulation to generate a highly linear ramp signal and perform the histogram test. A space decomposition technique is proposed for the A/D converters linearity test in [61]. While the original

histogram-based test collects the histogram of one code in the entire period, the proposed technique in [61] captures the output codes at around one point. In this way, the test time can be reduced as compared to the original histogram test. Since the above proposed methods are still based on the histogram method, all of the proposed methods require collecting a large number of samples and generating high-precision ramp signals for high-precision A/D converters. Linearity tests using the linear modeling technique are discussed in [24]-[27]. The test time can be reduced by measuring only a defined subset of transition levels, which is much less than the number of measurements required in the histogram-based test. However, the issue associated with the generation of high-resolution and linear signal source is still remained.

The long test time as a result of large measurement and/or the generation of high-precision input stimuli are associated with the above proposed techniques. As a result, methodologies using lower resolution input stimuli than the A/D converters under test and/or collecting less output samples than the histogram test are explored in the past. An estimation of the static performance from the spectrum analysis is studied in [62] – [63]. In [62], the authors use FFT to measure INL of the A/D converters with resolutions of 16-bit to 20-bit. The INL is derived using Chebyshev polynomials. The coefficients of the polynomials are defined from the spurious harmonics of the spectrum output. The authors in [63] use the fact that capacitor mismatch is the main source of the A/D converters nonlinearity. The capacitor mismatch is predicted from harmonic distortion measurements, and the authors form a connection between INL and harmonic distortions. Concerns with spectrum analysis must be considered. In [8]-[12], the authors propose to use dynamic

element matching (DEM) and deterministic dynamic element matching (DDEM) methods for the histogram testing of high-resolution A/D converters using non-linear D/A converters. These methods reduce or eliminate the non-linearity of the D/A converters before applying them to the A/D converters under test. As a result, the test stimuli with lower resolutions than the A/D converters under test can be applied to the devices under test (DUTs). The authors in [13]-[15] propose the linearity test using imprecise stimulus, and these works are led to [16]-[17]. In [16]-[17], a stimulus error identification and removal (SEIR) technique is proposed to compensate for the non-linearity present in the input test stimulus. Two identical sets of input signals are shifted by an offset voltage and are applied to the A/D converters. This technique is also based on the histogram test method, but the technique requires collecting much less output samples than the original histogram test. The required number of samples is approximately the total number of digital codes of the A/D converters under test. The non-linearity of imprecise analog input signal is identified and removed at the end. The technique reduces the number of samples to collect compared to the original histogram test, but this reduced number of samples is still large, and the technique requires an effort of building appropriate filters such as a low-pass filter (LPF) or band-pass filter (BPF) at the output of the D/A converters to generate smooth signals.

4.2. PROPOSED METHODOLOGY

The proposed methodology is developed to test the high-resolution A/D converters using low-precision D/A converters. In the proposed methodology, a low-precision D/A converter and a potentiometer are used for generating a test stimulus to the high-resolution A/D converters under test. The methodology is based on a least-squares polynomial-fitting technique and estimates the transfer function of the A/D converters by taking output code measurements made at intermediate code points. The test setup and analysis procedure make no assumption about the linearity of the low-precision D/A converters or low-precision input stimuli. The computed transfer function is used to estimate the INL and DNL of the system accurately. The methodology can be applied to any architecture of the A/D converters. However, the methodology is efficient especially for the high-precision A/D converters, which have 18-bit to 24-bit resolution such as successive approximation register (SAR), sigma-delta, and incremental A/D converters. Chapter 4.2.1 presents the proposed methodology.

4.2.1 Implementation of Proposed Methodology

The Chapter 4.2.1 describes a detail implementation of the proposed methodology. A brief introduction of the approach with core concept is described in Chapter 4.2.1.1, and Chapter 4.2.1.2 illustrates the proposed test setup and test flow. Then, data analysis and

mathematical formulation are explained in Chapter 4.2.1.3. An improved technique is added in Chapter 4.2.1.4.

4.2.1.1 Core Concept

A core concept of the proposed methodology is described in Section 4.2.1.1. The proposed linearity testing methodology allows the least-squares-fitting technique to estimate the transfer function of the high-resolution A/D converters numerically. Figure 1 in Chapter 1.1.1.1 presents the transfer function of an ideal 3-bit A/D converter. As described in Chapter 1.1.1, a *code width* of the A/D converter is defined as a range of a set of analog input voltage values that correspond to a single digital code, while a *code transition point* is a point of the analog signal value at which a digital code transitions from one code to the next code. Consequently, the transfer function of the A/D converter forms a many-to-one mapping relationship between analog input signal values and digital output codes. However, this transfer function with the many-to-one mapping is described by an one-to-one mapping function in the proposed methodology. This one-to-one mapping function is expressed as a code transition point (analog signal transition point) versus a digital code. In case of the ideal A/D converter transfer function, all code transition points fall along a straight line as shown in Figure 1. Accordingly, all the code widths of the ideal A/D converter are equal to each other. In the proposed method, the digital output code and analog input signal are defined as “y” and “x”, respectively. The transfer function of the A/D converter denoted by “f” maps the analog input “x” to its corresponding digital code

"y" and is expressed as y=f(x). For the ideal A/D converter, the digital codes are given by y=k*x, where k is a constant that represents the gain of the A/D converter. Since all the digital codes of the ideal A/D converter have the equal code widths, all code widths shown in Figure 1 are $1/8^{th}$ of the A/D converter full-scale voltage reference. However, all code widths are not equal in reality due to manufacturing imperfections generating non-linearity. These manufacturing imperfections lead to a non-linear transfer function of y=f(x), and this non-linear transfer function cannot be depicted by the straight line shown in Figure 1. The non-linear transfer function of y=f(x) can be parameterized by a set of basis functions. A polynomial function is used as the basis function in this methodology, but other forms of basis functions can also be studied and applied.

4.2.1.2 Proposed Test Setup and Test Flow

The proposed linearity test setup is shown in Figure 80. The proposed method uses two D/A converters (or potentiometers) with an M- bit resolution and an L-bit resolution to test an N-bit resolution A/D converter. For the purpose of using low-precision and low-cost input signals in the proposed approach, the resolution N is much bigger than the resolutions of M and L (L >> M, L). Note that the resolution M needs not be the same as the resolution L. An analog output signal range of the M-bit D/A converter is assumed to have the equal full-scale range of the analog input of the N-bit A/D converter under test. This assumption allows the proposed technique to cover the full-scale range of the DUT (N-bit resolution A/D converter). While the M-bit D/A converter generates a set of analog input voltage

values for the A/D converter under the test, the L-bit D/A converter is used to generate a set of offset voltage values, which scales the output of the M-bit D/A converter. Each set of analog output voltage from the M-bit D/A converter can be described as a ramp signal, and the offset voltage values of the L-bit D/A converter are controlled by setting the digital values of a L-bit register. Then, each scaled set of analog voltage values from the M-bit and L-bit D/A converters is applied to the N-bit resolution A/D converter under test. For a pre-determined offset voltage generated by the L-bit D/A converter, a set of digital codes is applied to the M-bit D/A converter, and the corresponding codes obtained at the output of the A/D converter under test are recorded. For the maximum use of the M-bit D/A converter, all the possible digital codes of the D/A converter are used in the proposed methodology. This process is repeated until sufficient data are obtained for the linearity analysis of the A/D converter under test.

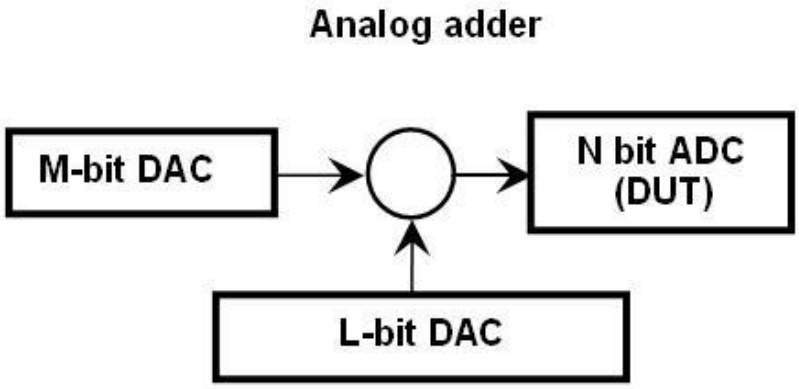

Figure 80. Linearity Test Setup

In the proposed methodology, two identical sets of digital codes are applied to the M-bit D/A converter for different offset voltage values generated by the L-bit D/A converter, so two identical analog signal sets are present at the input of the analog adder for each offset voltage as shown in Figure 80. Here, two offset voltage values, a zero and a non-zero, are used. It is assumed that the noise performance of the M-bit and L-bit D/A converters can be compensated through repeated tests. The noise effect can be reduced or removed by averaging the data from the repeated tests. Note that 2^M analog input signals can be applied to the A/D converters with the second offset voltage depending on the value of the offset voltage selected. All the output data from the M-bit D/A converter and L-bit D/A converter are assumed to be unknown in this methodology. The reason for such assumption is because the N-bit A/D converter under test is extremely high-precision converter and is too sensitive to an extremely small voltage value, which may not be possible to be measured accurately. Therefore, only information available in this methodology is the digital output code measurement from the N-bit A/D converter under test.

4.2.1.3 Data Analysis and Mathematical Formulation

The transfer function of the A/D converter under test is expressed mathematically as y=f(x). Conversely, since the one-to-one mapping between digital output codes and analog input transition points is assumed in the proposed methodology, a polynomial function of "g", where $g=f^{-1}$, is defined to map the digital code "y" back to its corresponding analog input voltage "x". Such a mapping can be expressed mathematically as x=g(y). In this

methodology, the polynomial function maps a given output code of the A/D converter to a corresponding valid input transition voltage. The objective is to determine this polynomial function as accurately as possible from the collected test dataset. Note that the inverse transfer function of "g" is computed instead of "f" because this facilitates direct analysis of the test data. The obtained inverse transfer function of "g" at the end of the test procedure is used to compute the direct transfer function of "f". Equation 20 defines the inverse transfer function, "g", of the A/D converter as the polynomial function with a degree 'p', where i=0,1,2,,,,(2^M-1), and M is the resolution of the M-bit D/A converter. The polynomial equation gives all the code transition points (x_i) for normalized digital codes (y_i). The transfer function with the polynomial coefficients of α_1 to α_p determines the linearity of the A/D converter under test.

$$x_i = g(y_i) = \sum_{j=1}^{p} \alpha_j {y_i}^j = f^{-1}(y_i) \qquad \text{Equation 20}$$

The goal of the test procedure is to determine the polynomial coefficients precisely from the test response measurements corresponding to the two offset voltage values, which are applied by the L-bit D/A converter. For a given offset voltage Δ, the set of all digital codes of the M-bit D/A converter is denoted as a test suite TS(Δ), where Δ is the difference between two offset voltage values. Since a zero voltage and a non-zero voltage are used as two offset voltage values, Δ is equal to the non-zero offset voltage. In the proposed approach, two such test suites, TS(o) and TS(Δ), are applied with offset voltages of 0 and Δ, respectively. Each test suite consists of 2^M digital codes for the M-bit D/A converter.

The transfer function of the A/D converter under test with two sample measurement is shown in Figure 81. Let $x_i(0)$ and $x_i(\Delta)$ denote the analog voltage values generated by a digital code 'i' from the test suites TS(0) and TS(Δ), respectively. The digital codes that correspond to the analog voltage values of $x_i(0)$ and $x_i(\Delta)$ are denoted by $y_i(0)$ and $y_i(\Delta)$, respectively. Then, from Equation 20, the analog voltage values can be expressed mathematically as follows:

$$x_i(o) = g(y_i(o)) = \alpha_1 y_i(0) + \ldots + \alpha_p y_i{}^p(0) \qquad \text{Equation 21}$$

$$x_i(\Delta) = g(y_i(\Delta)) = \alpha_1 y_i(\Delta) + \ldots + \alpha_p y_i{}^p(\Delta) \qquad \text{Equation 22}$$

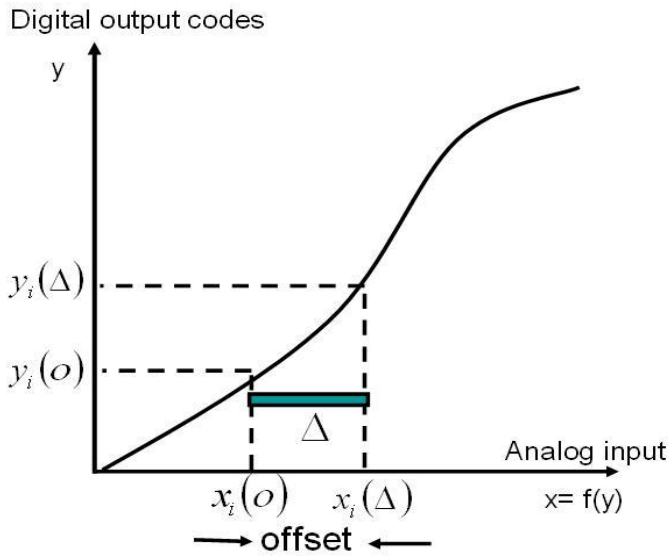

Figure 81. Transfer function with two samples

It should be noted that $x_i(0)=x_i(0) + \Delta$. Based on this property, Equation 23 is constructed for a given digital code 'i' of the D/A converter from Equation 21 and 22.

$$x_i(\Delta) - x_i(o) = \Delta = \sum_{j=1}^{p} \alpha_j \left(y_i(\Delta)^j - y_i(o)^j \right) \qquad \text{Equation 23}$$

For all possible values of 'i' from 0 to 2^M-1, several such equations can be constructed by measuring the corresponding digital codes. The key concept is that the difference between $y_i(0)$ and $y_i(\Delta)$ is different due to the non-linearity of the A/D converter for different values of 'i' although the offset voltage value Δ is fixed throughout the entire experiment. This difference between $y_i(0)$ and $y_i(\Delta)$ would remain same with the fixed offset value of Δ for the ideal A/D converters that do not include the non-linearity. The coefficients of α_j, where $1 \le j \le p$, can be computed easily by solving the over-constrained system of equations using the least-squares-fitting method. For success of such technique, the offset voltage Δ needs to be measured accurately with the N-bit precision, which defeats the purpose of developing a low-cost test solution in this proposed methodology. Hence, the value of Δ is assumed to be unknown, and the unknown Δ makes the direct computation of the coefficients impossible from Equation 23.

To address the above issue, the use of scaling method is proposed in this thesis to solve for the coefficients of the A/D converter. Equation 24 shows the matrix representation of the over-constrained set of equations obtained from Equation 23. The matrix in Equation 23 has a form of $A\alpha = \Delta$, where Δ is unknown. A known scalar value of b such that $b = \gamma\Delta$ is defined, where b represents the scaled value of Δ. Instead of solving for $A\alpha = \Delta$, solving $A\alpha' = b$ results in a set of coefficients α' such that $\alpha' = \gamma\alpha$. For a well conditioned matrix A, the α' can be computed using a simple inversion operation as given by $\alpha = (A^T A)^{-1} A^T b$.

Alternatively, the matrix can also be solved numerically to obtain α'. If γ is known, then α can be obtained by scaling back α'.

$$\begin{bmatrix} (y_0(\Delta)-y_0(o)) & \cdots & (y_0^p(\Delta)-y_0^p(o)) \\ (y_1(\Delta)-y_1(o)) & \cdots & (y_1^p(\Delta)-y_1^p(o)) \\ \vdots & \cdots\ \cdots & \vdots \\ (y_{(2^M-1)}(\Delta)-y_{(2^M-1)}(o)) & \cdots & (y^p_{(2^M-1)}(\Delta)-y^p_{(2^M-1)}(o)) \end{bmatrix} \begin{bmatrix} \alpha_1 \\ \alpha_2 \\ \vdots \\ \alpha_p \end{bmatrix} = \begin{bmatrix} \Delta \\ \Delta \\ \vdots \\ \Delta \end{bmatrix}$$

Equation 23

The analog signal x'_i that corresponds to a set of coefficients α' can be represented mathematically by Equation 24.

$$x'_i = \sum_{j=1}^{p} \alpha'_j y_i^{\,j} = \gamma \sum_{j=1}^{p} \alpha_j y_i^{\,j} = \gamma x_i \qquad \text{Equation 24}$$

For i = 2^M-1, x_i corresponds to the full-scale (FS) voltage of the N-bit A/D converter. Once the α'_j are obtained, the analog signal voltage of x'_{2^M-1} can be obtained from Equation 24, which corresponds to a digital code at i=2^M-1. Then, the value of γ can be computed using Equation 25.

$$\gamma = \frac{x'_{2^M-1}}{FS} \qquad \text{Equation 25}$$

Once γ is calculated, the α' can be scaled back to its original value of α to define the overall transfer function of the A/D converter under test. The resolution of the M-bit D/A converter is not necessarily high, but the accuracy of the proposed method depends on the resolution of the M-bit D/A converter and the number of samples collected to construct the over-constrained system of Equation 23. This scaling technique works relatively well, but the technique still faces with an accuracy issue in some cases: the accuracy limitations of estimating millions of points for the high-resolution A/D converters with only one basis function and a coarse D/A converter. Having high-degree of a polynomial basis function cannot solve this issue since the high-degree polynomial function may lead to an over-fitting problem. The degree of the polynomial function must be carefully determined to avoid the over-fitting problem. For the given number of samples, the accuracy of the technique can be further enhanced by segmenting the overall transfer function into several segments and solving for the polynomial transfer function for each segment. This technique, which is called segmentation, is described in Chapter 4.2.1.4.

4.2.1.4 Segmentation Method

The Section 4.2.1.4 introduces a technique called segmentation technique that improves the accuracy of estimation from the previous scaling method in Chapter 4.2.1.3. Figure 82 describes the segmentation methodology. In the segmentation technique, the overall transfer function in a full-scale range of the A/D converter is divided into several windows or segments as shown in Figure 82. Instead of finding one basis polynomial function for the

entire full-scale range, the segmentation technique finds a basis function for each segmented window. For each window, the previous scaling method is used to solve for the polynomial coefficients that define the transfer function in that specific window. In Figure 82, the overall transfer function in the full-scale range is divided by a set of T windows from W_1 to W_T. For success of this segmentation technique, the number of windows 'T' needs to be chosen carefully to ensure that sufficient number of measurement samples exist for each window to solve for the polynomial transfer function.

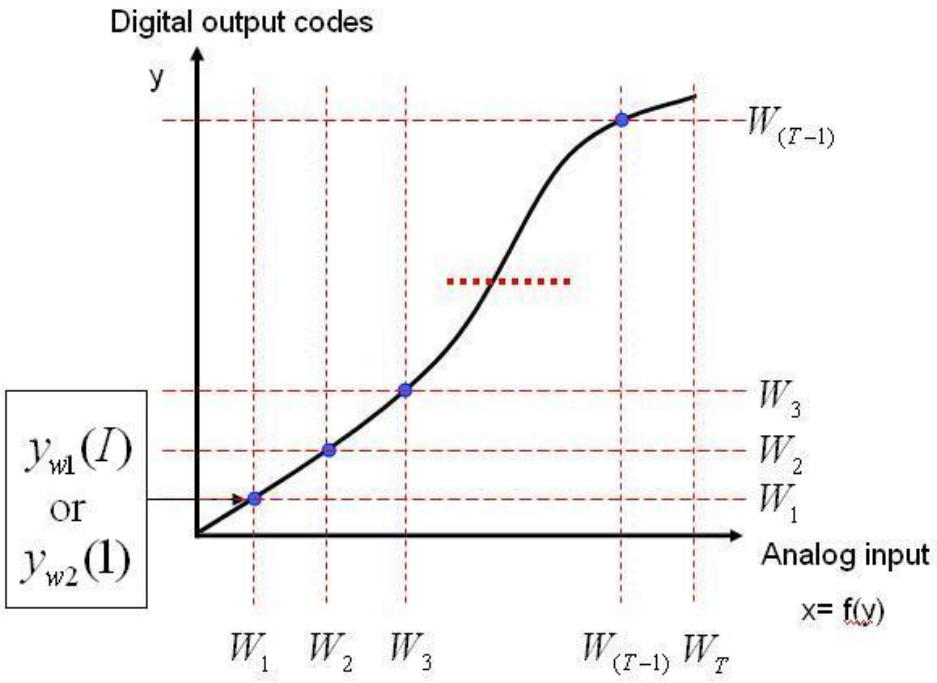

Figure 82. Segmentation of transfer function.

For simplicity, the proposed segmentation method is explained using two windows of W_1 and W_2, and the properties of the windows W_1 and W_2 are summarized as follows:

1. A window W_1 contains a set of digital codes as $Y_{w1} = \{y_{w1}(1), y_{w1}(2), \ldots, y_{w1}(I)\}$.
2. A polynomial equation in W_1 generates analog input voltage of
   $X_{W1} = \{x_{w1}(1), x_{w1}(2), \ldots, x_{w1}(u)\}$.
3. A window W_2 contains a set of digital codes as $Y_{w2} = \{y_{w2}(1), y_{w2}(2), \ldots, y_{w2}(J)\}$.
4. A polynomial equation in W_2 generates analog input voltage of $X_{W2} = \{x_{w2}(1), x_{w2}(2), \ldots, x_{w2}(h)\}$.

To ensure a smooth transition from one window to the next window, two key boundary conditions should be satisfied as seen in Figure 83. Figure 83 shows how the transfer functions in two windows can be matched and continuous. First, the end digital code, $y_{w1}(I)$, in window W1 must be the same as the first digital code, $y_{w2}(1)$, in window W2. Second, the analog voltage values of $x_{w1}(u)$ and $x_{w2}(1)$ that correspond to the digital codes of $y_{w1}(I)$ and $y_{w2}(1)$ must be identical. However, the analog voltages "x" computed for the same code of $y_{w1}(I)$ and $y_{w2}(1)$ need not be the same and depend upon the accuracy of computation of the transfer function polynomials, i.e. $x_J^{W_1} \neq x_1^{W_2}$. To resolve such issue, subtracting all calculated code transition points of the second window, X_{W2}, from the difference of $x_{w2}(1) - x_{w1}(u)$ is proposed. In this way, the $x_J^{W_1} = x_1^{W_2}$ can be obtained as shown in Figure 83below. Note that the subtraction value of $x_{w2}(1) - x_{w1}(u)$ is one possible solution used in this proposed methodology, and $x_{w1}(1) - x_{w2}(u)$ or a value between $x_{w2}(1) - x_{w1}(u)$ and $x_{w1}(1) - x_{w2}(u)$ in a random manner for each window can be also used. In fact, the analysis of all above three possible approaches demonstrates in simulation environment that one approach does not differ much from another approach. In the following Chapter 4.3, the software simulation results are discussed.

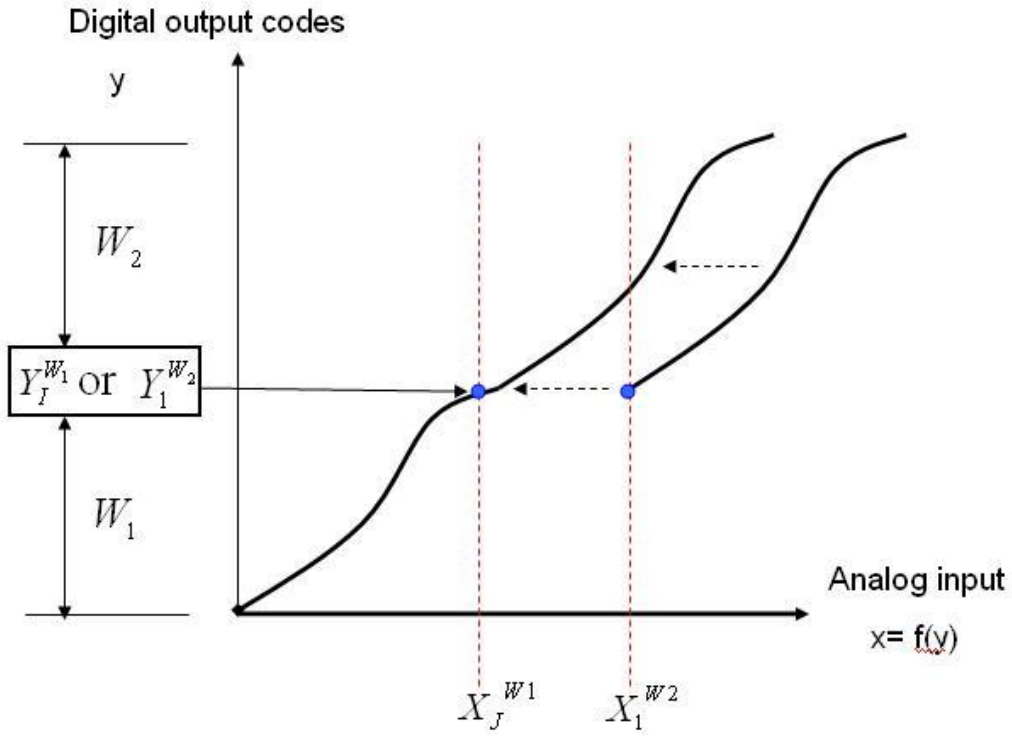

Figure 83. Matching transfer function in two windows.

4.3. SIMULATION RESULTS FOR VALIDATION

Matlab simulation results for testing 24-bit and 18-bit A/D converters using two 10-bit D/A converters (potentiometers) are presented. The 10-bit D/A converter was modeled after Max5495, which is a two-channel 10-bit digital potentiometer from Maxim. This 10-bit resolution Max5495 will be used to generate the offset voltage in the hardware experiment.

The INL and DNL specifications of the 10-bit D/A converter from the datasheet of Max5495 are shown in Figure 84, and its Matlab model with noise is shown in Figure 85.

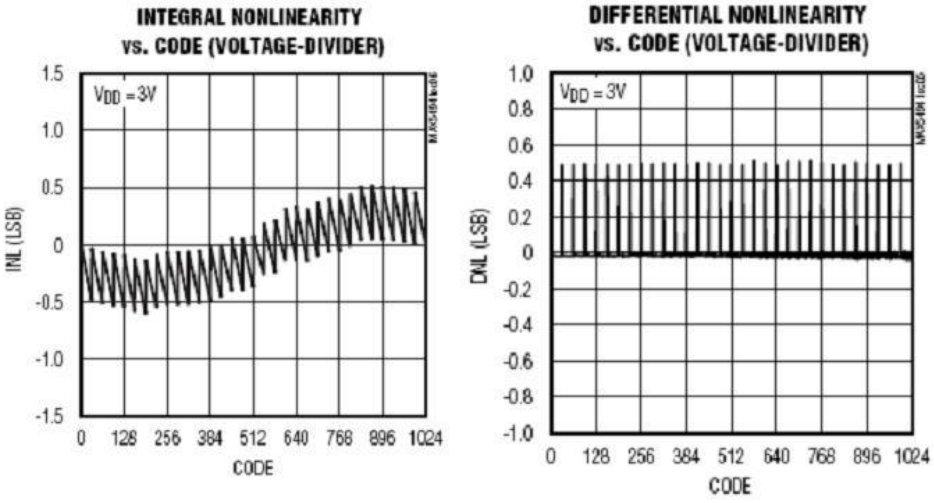

Figure 84. INL and DNL plots of Max5495 from datasheet

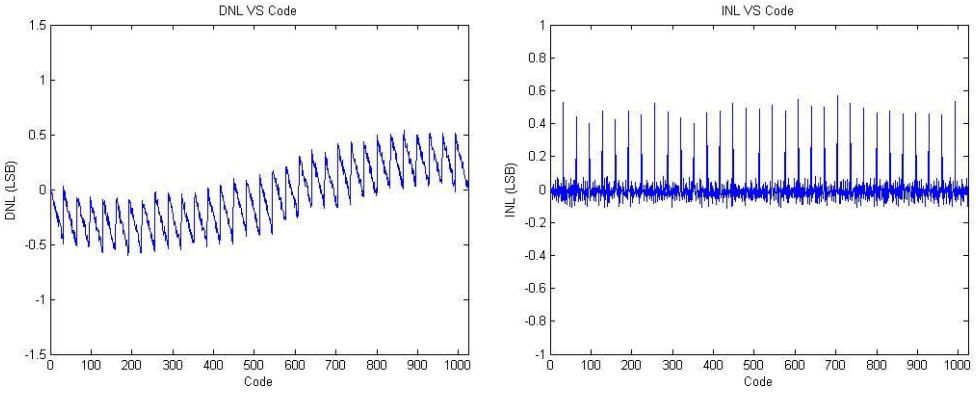

Figure 85. Modeling of Max5495

The proposed technique was validated for various shapes of the A/D converters transfer functions. To average out the effect of the data converter noise, each digital code was repeated 128 times (128 repeated tests), and the average digital code values were used as the test data for both the 24-bit and 18-bit D/A converters. The proposed methodology was validated on three different models of the A/D converters varying degree of non-linearity in this software experiment.

First, the INLs of the three A/D converter models under test were estimated using the only scaling technique (with no segmentation technique). Since DNL plots can be estimated from INL plot once the transfer functions of the converters are obtained, only INL plots are provided here to avoid redundancy. The comparison plots between the actual non-linearity and the estimated non-linearity generated by software simulation are presented in Figure 86 - Figure 88. In Figure 86 - Figure 88, the simulation results without the segmentation technique are provided when using different degrees of the polynomial basis function. The estimation results in Figure 86 - Figure 88 are the best INL estimations after trying various degrees of the polynomial functions. From the simulation results, the accuracy of INL estimations for all three 18-bit A/D converter models was the best with 8^{th}-order polynomial functions, while lower degree polynomial functions than 8^{th}-order should be used for the 24-bit A/D converters to avoid the over-fitting problem. Polynomial functions with higher degree than 8^{th}-order and 6^{th}-order resulted in the over-fitting problem for the 18-bit A/D converters and 24-bit A/D converters, respectively, leading to bad estimations. However, the results in Figure 86 - Figure 88 are not accurate enough, especially for the 24-

bit precision cases, and the INL errors are not acceptable values. These estimations can be improved using the scaling and segmentation techniques together.

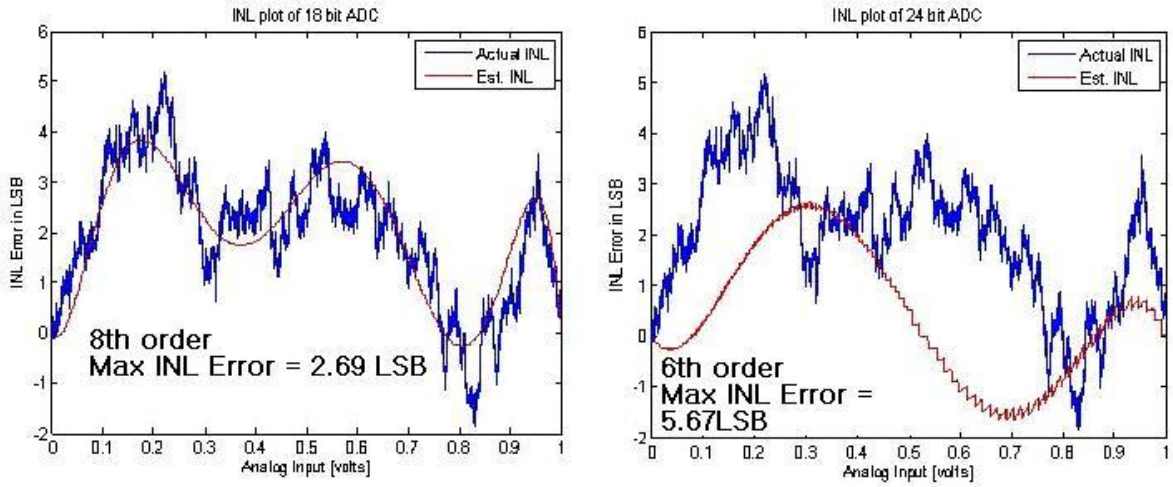

Figure 86. INL plots for A/D converter model 1 with no segmentation technique: 18-bit resolution in left and 24-bit resolution in right

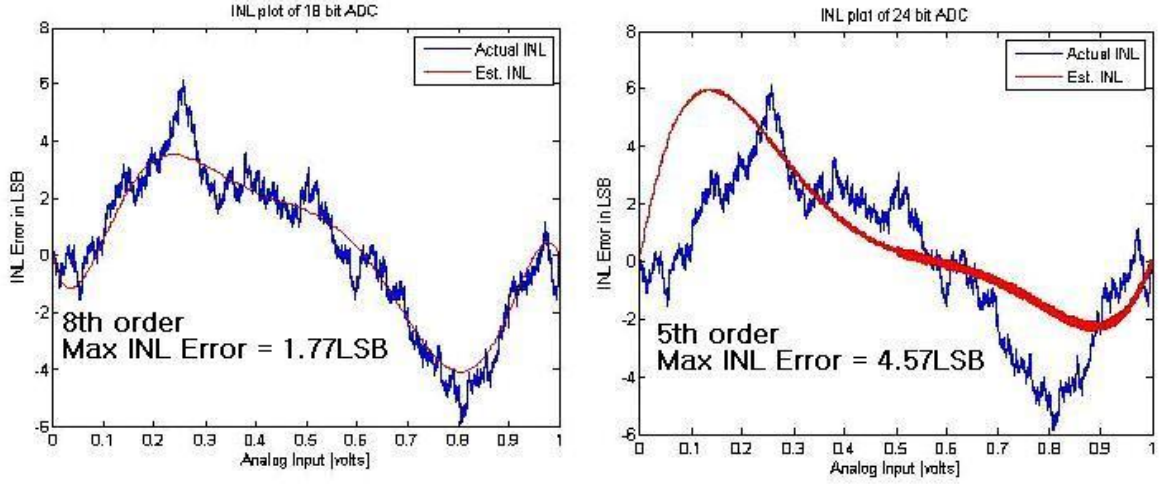

Figure 87. INL plots for A/D converter model 2 with no segmentation technique: 18-bit resolution in left and 24-bit resolution in right

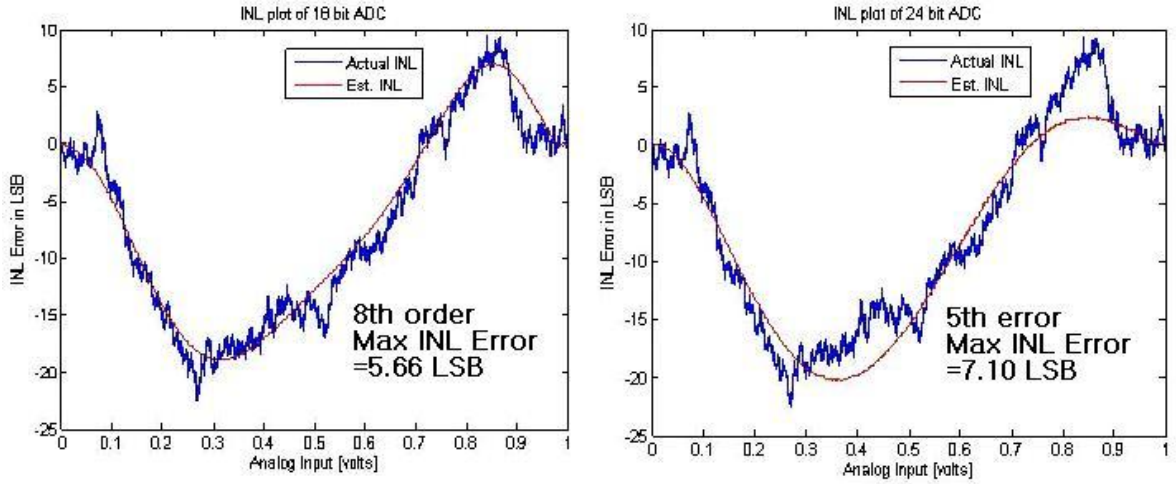

Figure 88. INL plots for A/D converter model 2 with no segmentation technique: 18-bit resolution in left and 24-bit resolution in right

The INLs of the identical A/D converters with 18-bit and 24-bit resolutions were estimated using both the scaling and segmentation techniques together. The value of the offset voltage Δ was fixed at 10 LSB of the 10-bit potentiometer in this experiment (10 LSB = code number 10 of possible codes 0 to 1023). In all cases, a 2^{nd}-order polynomial basis function was used for each window. The comparison plots between the actual and the estimated non-linearity are shown in Figure 89 to Figure 97 for the three different values of the total number of windows 'T', which are 10, 50, and 100 windows. Test results using the scaling and segmentation methods describing Figure 89 to Figure 97 are summarized in Table 8.

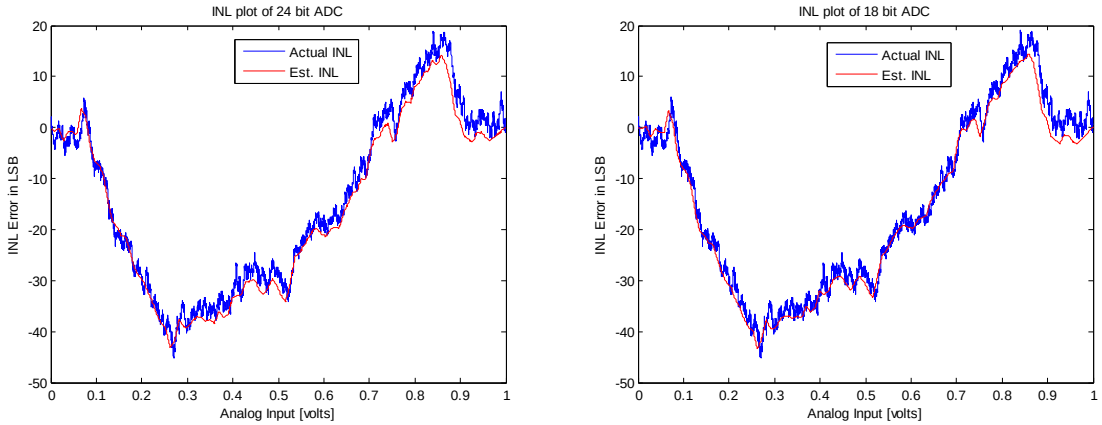

Figure 89. INL plots using 100 windows: model 1 with 24-bit resolution in left and 18-bit resolution in right.

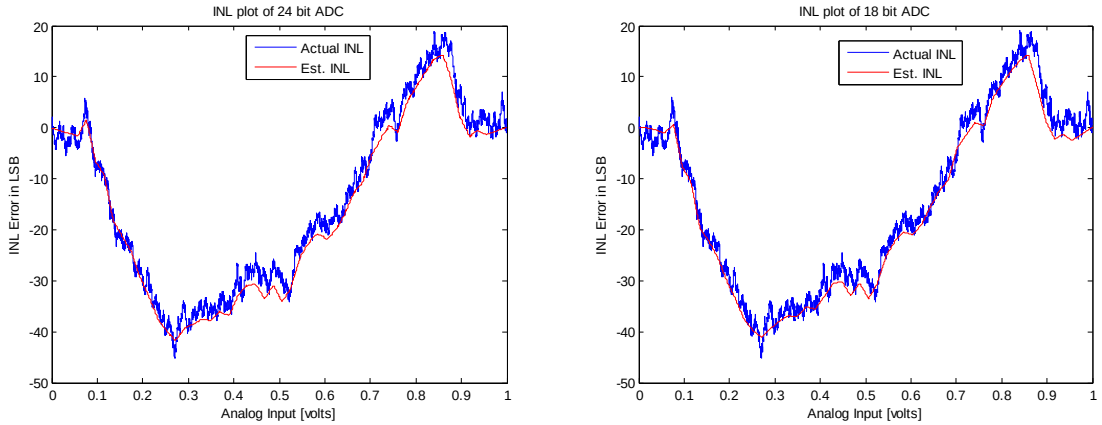

Figure 90. INL plots using 50 windows: model 1 with 24-bit resolution in left and 18-bit resolution in right.

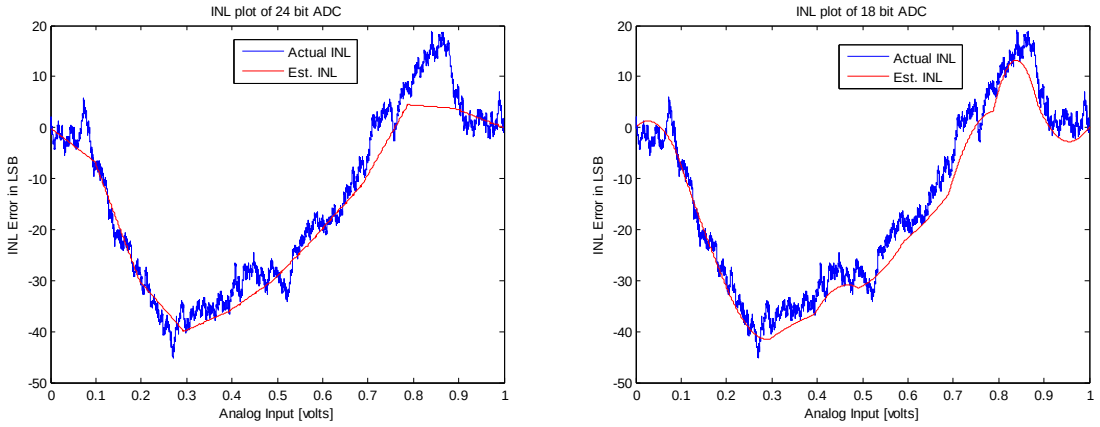

Figure 91. INL plots using 10 windows: model 1 with 24-bit resolution in left and 18-bit resolution in right.

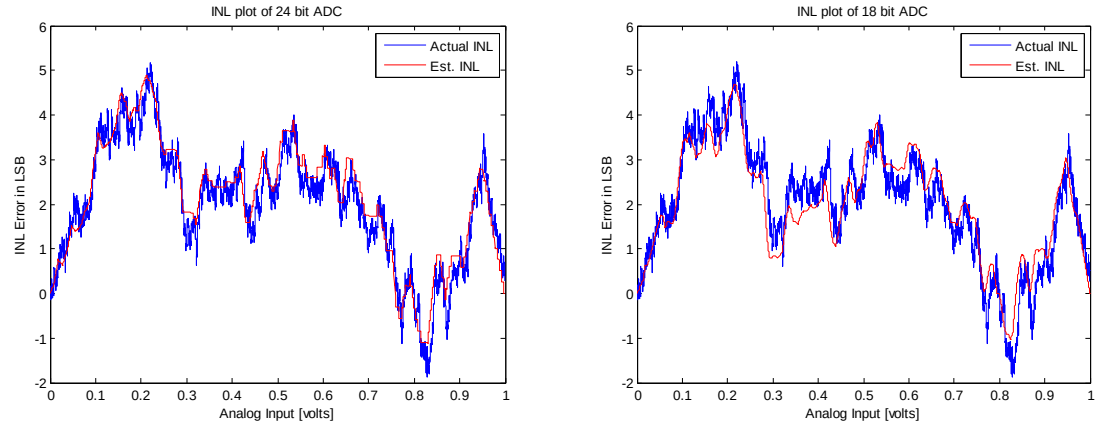

Figure 92. INL plots using 100 windows: model 2 with 24-bit resolution in left and 18-bit resolution in right.

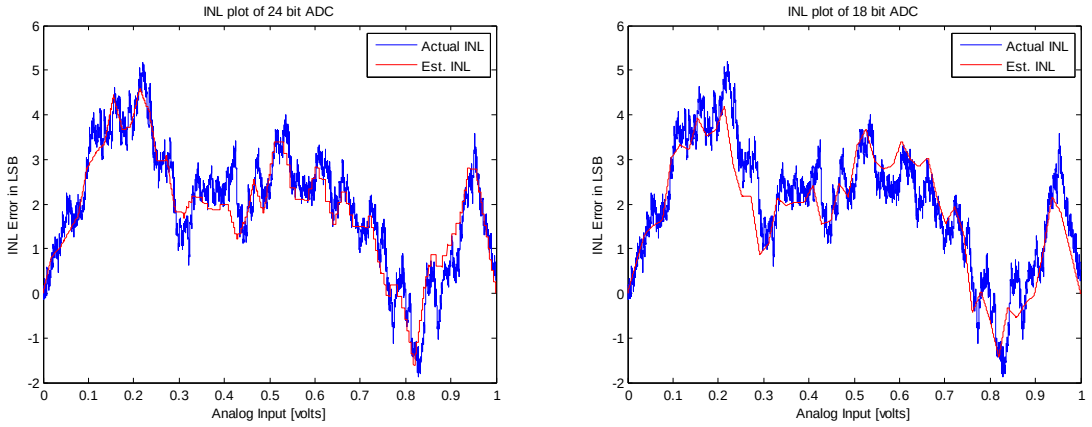

Figure 93. INL plots using 50 windows: model 2 with 24-bit resolution in left and 18-bit resolution in right.

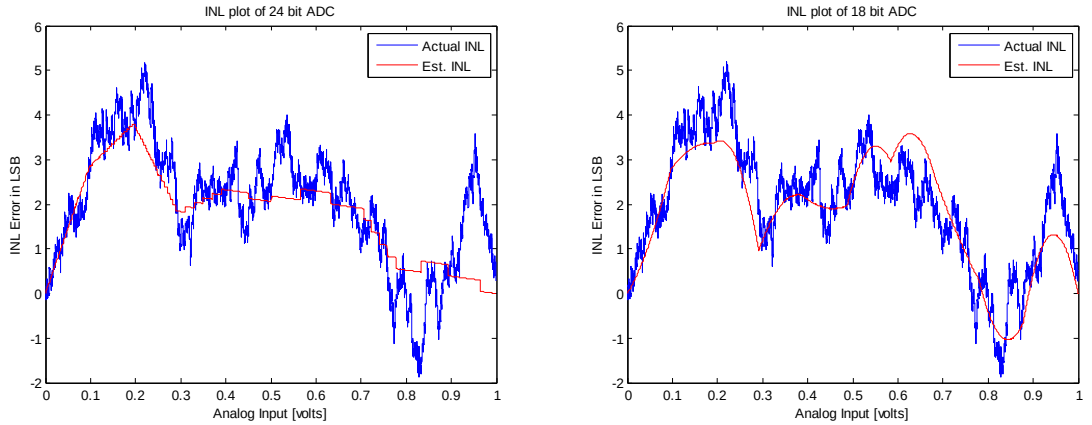

Figure 94. INL plots using 10 windows: model 2 with 24-bit resolution in left and 18-bit resolution in right.

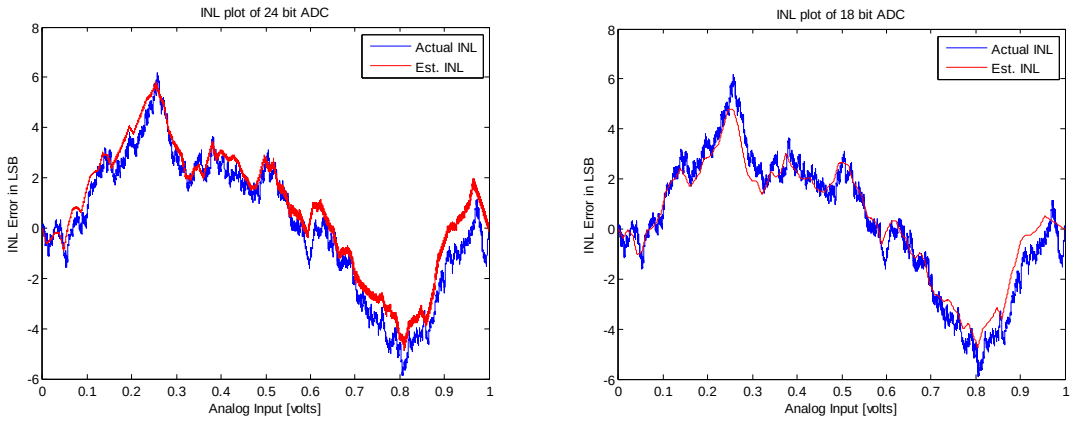

Figure 95. INL plots using 100 windows: model 3 with 24-bit resolution in left and 18-bit resolution in right.

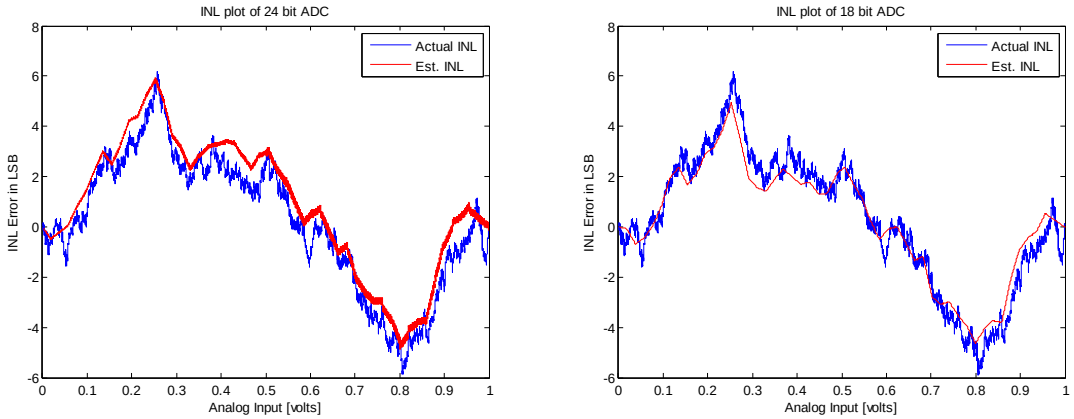

Figure 96. INL plots using 50 windows: model 3 with 24-bit resolution in left and 18-bit resolution in right.

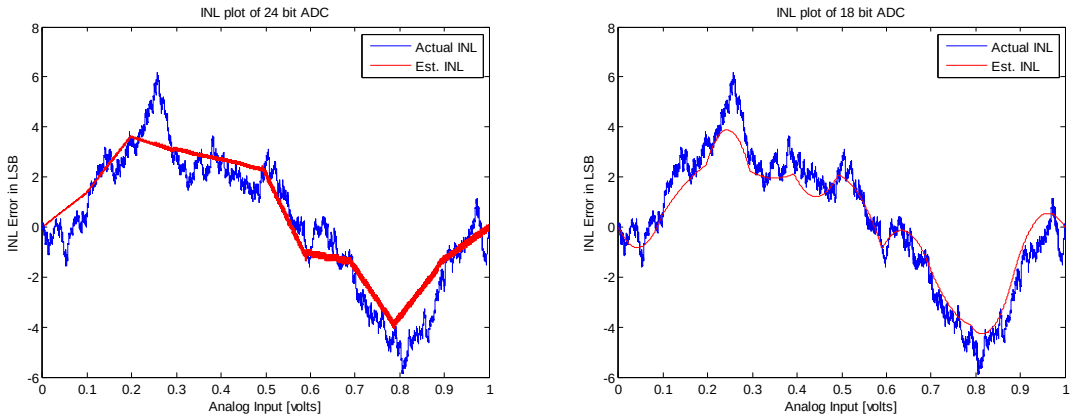

Figure 97. INL plots using 10 windows: model 3 with 24-bit resolution in left and 18-bit resolution in right.

Table 8. Summary of simulation results.

	A/D converters	Number of windows	Polynomials	Max. INL error
18 Bit	Model 1	10	2^{nd}-order	5.4 LSB
		50	2^{nd}-order	3.2 LSB
		100	2^{nd}-order	1.86 LSB
	Model 2	10	2^{nd}-order	1.88 LSB
		50	2^{nd}-order	1.64 LSB
		100	2^{nd}-order	0.92 LSB
	Model 3	10	2^{nd}-order	2.4 LSB
		50	2^{nd}-order	1.3 LSB
		100	2^{nd}-order	0.86 LSB
24 Bit	Model 1	10	2^{nd}-order	8.24 LSB
		50	2^{nd}-order	3.6 LSB
		100	2^{nd}-order	2.4 LSB
	Model 2	10	2^{nd}-order	1.74 LSB
		50	2^{nd}-order	1.5 LSB
		100	2^{nd}-order	0.66 LSB
	Model 3	10	2^{nd}-order	2.61 LSB
		50	2^{nd}-order	2 LSB
		100	2^{nd}-order	0.95 LSB

The proposed methodology works well for both the 18-bit and 24-bit A/D converters as the simulation results show. The more segmentation windows the technique uses, the better estimation the technique can get**.** Figure 89 to Figure 97 observe that the estimated values closely track the actual non-linearity plots, and the estimations using the scaling technique only are significantly improved with the scaling and segmentation techniques together. The errors in estimation can be improved by using D/A converters with higher resolution (12-bit to 14-bit) or averaging out more data. The most meaningful test improvement is that only 262,144 samples were taken to estimate the non-linearity of the 24-bit and the 18-bit A/D converters in comparison to the conventional histogram test, which requires more than 480 million samples to test a 24-bit A/D converter with an average of 30 samples per a code. Table 9 summarizes the comparison results of maximum INL errors that can be achieved with the histogram test and the proposed test. As shown in Table 9, the proposed test can achieve much more accurate INL measurements with the significantly reduced number of output measurements as compared to the conventional histogram test. A common 24-bit ADC has an output data rate (ODR) of less than a few mega samples per second (SPS). When a 24-bit ADC with ODR of 4M SPS is tested by the histogram test with an average number of 30 samplers per a code, the total test time for collecting the output samples will be 125.8291 second (503,316,480 output measurements) as compared to only 0.0512 second (204,800 output measurements) using the proposed test. In addition to the reduced test time as a result of reduced measurement compared to the histogram test, the use of low-cost test equipment can reduce the cost of testing. In addition to the reduced test time as a result of reduced measurement compared to the histogram test, the use of low-cost test

equipment can reduce the cost of testing. Figure 98 presents the test improvement using the proposed methodology.

Table 9. Comparison results between histogram test and proposed test.

		Histogram test		Proposed test	
	ADC under test	Number of output samples	Max. INL error	Number of output samples	Max. INL error
18-bit	Model 1	7,864,320	13.34 LSB	204,800	1.86 LSB
	Model 2	7,864,320	11.22 LSB	204,800	0.92 LSB
	Model 3	7,864,320	12.87 LSB	204,800	0.86 LSB
24-bit	Model 1	503,316,480	20.65 LSB	204,800	2.4 LSB
	Model 2	503,316,480	17.92 LSB	204,800	0.66 LSB
	Model 3	503,316,480	19.14 LSB	204,800	0.95 LSB

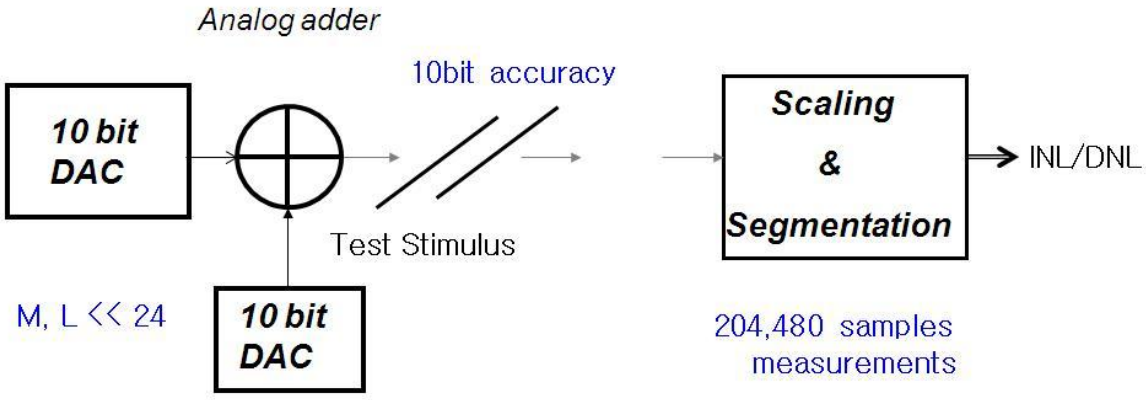

Figure 98. Test improvement with the proposed method.

Figure 99 presents allowable input resolutions that can be used to test the 24-bit ADC in the proposed methodology. The input signals with the identical INL and DNL shapes in Figure 85 were generated with various precisions and applied to the above 24-bit ADC 1 –

ADC 3. The maximum size of the input signal (2^M) was applied to the ADC under test, where M is the resolution of the input signal, and 2^{nd} order polynomial, 100 segmentations, and 10 LSB offset were used in the proposed test throughout the simulation experiments. Figure 99 shows that the lowest input resolution must be 10-bit or higher for testing the 24-bit ADCs with the proposed test. As the resolution of the input signal is increased, the accuracy is increased, and the number of measurements is also accordingly increased.

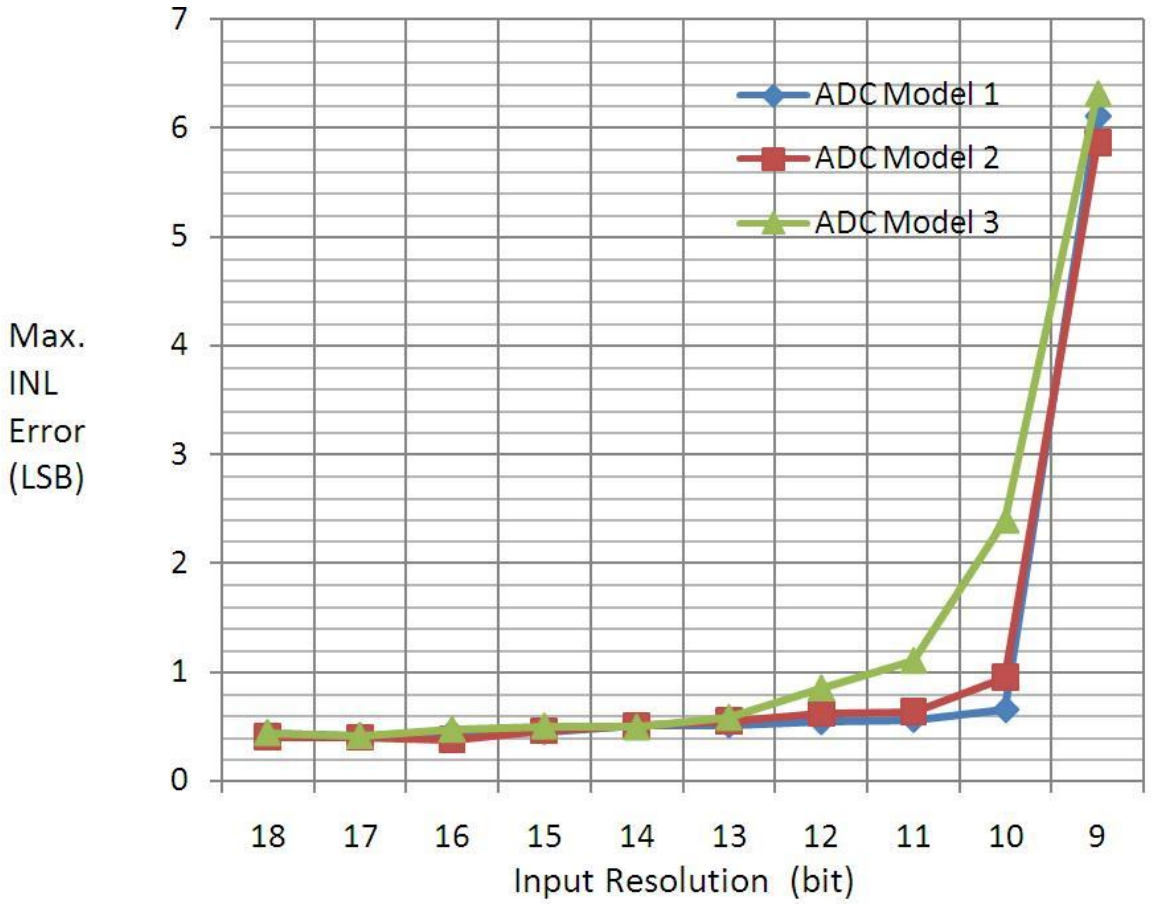

Figure 99. Input resolutions versus maximum INL errors.

4.4. VALIDATION OF PROPOSED METHODOLOGY

Hardware experiment was performed to validate the proposed linearity test. The proposed technique was developed for testing the high-precision A/D converters that have 18-bit or higher resolution. For the validation, the test result using the conventional histogram methodology must be needed as a reference and must be compared to the result of the proposed methodology. However, testing such high-resolution ADCs using the histogram test was difficult due to the lack of high-precision test facility that has the minimum resolution of 3-bit higher than A/D converters under test required by the conventional histogram test methodology. To test a 18-bit to 24-bit A/D converter, a 21-bit to 27-bit precision signal generator is required, and such precision signal sources are extremely expensive. As a result, the proposed test approach was validated by testing a set of 12-bit resolution A/D converters using a 10-bit resolution D/A converter and a 10-bit potentiometer s as a proof of the concept. This experiment setup validates the proposed test since the approach is capable of testing the A/D converters using lower-precision input source. Total number of the ADC set was 10 devices in this hard experiments.

4.4.1 Hardware Measurement Procedure

Figure 100 presents the test setup for the hardware experiment, which follows the test setup shown in Figure 80. In this experiment, the 10-bit D/A converter from Analog Devices (AD5310) was used as a ramp input signal generator, and the Max5495 10-bit

potentiometer from Maxim Integrated Products generated an offset voltage. Then, the offset voltage from Max5495 was added to the ramp input signal generated from AD5310 through ZFBT-6GWB bias tee from Minicircuits, which is used as an analog adder. Then, two scaled sets of ramp signals were applied to a set of 12-bit A/D converters under test (ADC121S101 from National Semiconductor). The data was acquired using Xilinx Spartan 3 FPGA based Nexys board from Digilent. In this experiment, 100 windows with 2^{nd}-order polynomial basis function were used with an offset voltage value of 10LSB of the 10-bit resolution potentiometer. Note that the maximum size of the two sets of the input voltage values (or maximum size of the corresponding digital output codes) is 2049 ($2x2^{10}$) for one test set. To compensate the noise effects of the 10-bit input signal, a test was reapeated 30 times for each ADC, and the output codes of 30 repeated test measurements were averaged out for each device. Therefore, the total number of output samples in the proposed test approach was 61,440 ($2x2^{10}x30$) for each device.

While the 10-bit precision signal stimulated the 12-bit resolution A/D converter under test in the proposed linearity test, the 14-bit resolution signal as the test input was generated using Agilent technology E4430B. This 14-bit signal might not be sufficient since the input requirement for testing 12-bit A/D converter is 15-bit precision theoretically, but the 14-bit source was the highest precision available in the lab facility, and it was assumed that the increased number of measurements might compensate for errors possibly occurred by 1-bit lower resolution source than required. Thus, the total length of 524,288 samples was collected to perform the histogram test, which is more than the average number of 100 samples per a code.

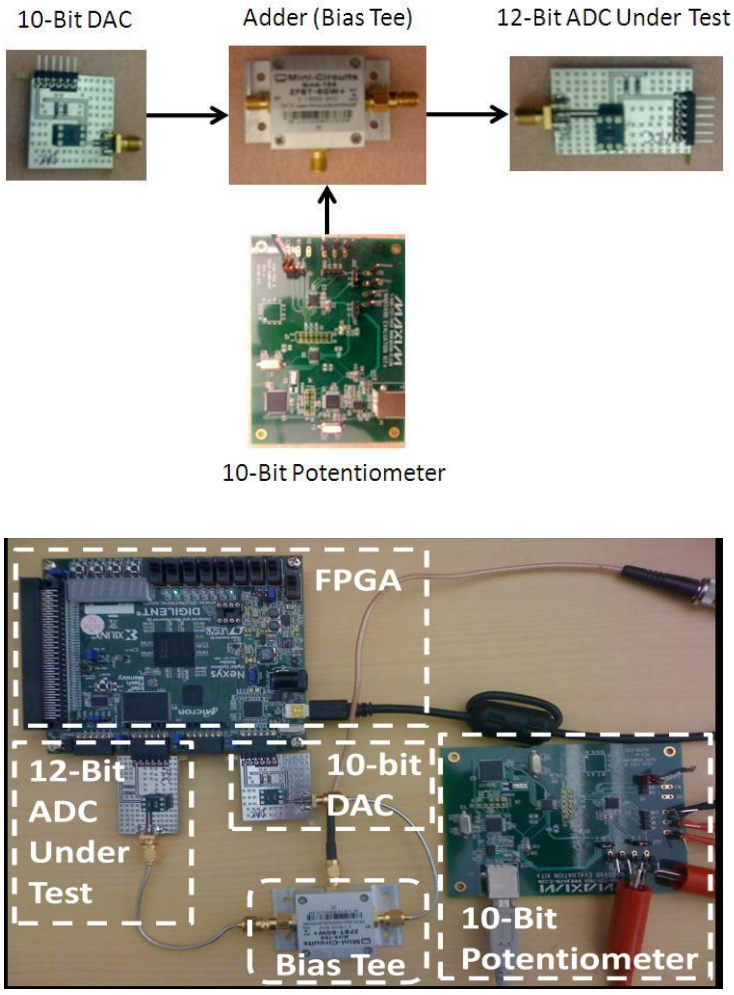

Figure 100. Test Setup for Hardware Validation.

4.4.2 Experimental Result

Following the measurement procedure explained in Chapter 4.4.1, the INLs of a set of 12-bit ADC121S101 was measured using the conventional histogram test and the proposed linearity test.

In the proposed test approach, the total number of samples collected was 61,440 ($2x2^{10}x30$), which is about 9 times less than the measurements (524,288) in the histogram test. The average number of samples per a code must be at least 30 samples per a code in the histogram, which implies 122,880 sample measurements, and the measurements of 61,440 samples in this approach is still less than 122,880 samples in the histogram.

Table 10 summarizes the maximum INL errors between the histogram test and the proposed test for the 10 ADCs (ADC121S101). All the maximum INL errors were less than 0.6451 LSB. This error can be further reduced if a higher input source is used or the output sample measurement is further increased.

Table 10. Maximum INL errors of 10 ADCs under test with the proposed test.

ADCs under test	Maximum INL error
ADC 1	0.4650 LSB
ADC 2	0.5128 LSB
ADC 3	0.4924 LSB
ADC 4	0.4671 LSB
ADC 5	0.4833 LSB
ADC 6	0.5801 LSB
ADC 7	0.5147 LSB
ADC 8	0.6451 LSB
ADC 9	0.4729 LSB
ADC 10	0.4872 LSB

Figure 101 presents the comparison of INL measurements using the histogram test and the propose test approach for the ADC 1 in Table 10. As seen in Figure 101, the INL measurement using the proposed methodology is as accurate as the INL measurement using

the histogram test, and both INL plots are well matched. This proposed approach characterizes the linearity of the A/D converter under test well using the lower-resolution source than the DUT and less measurements than the conventional test. The maximum INL error was 0.465LSB.

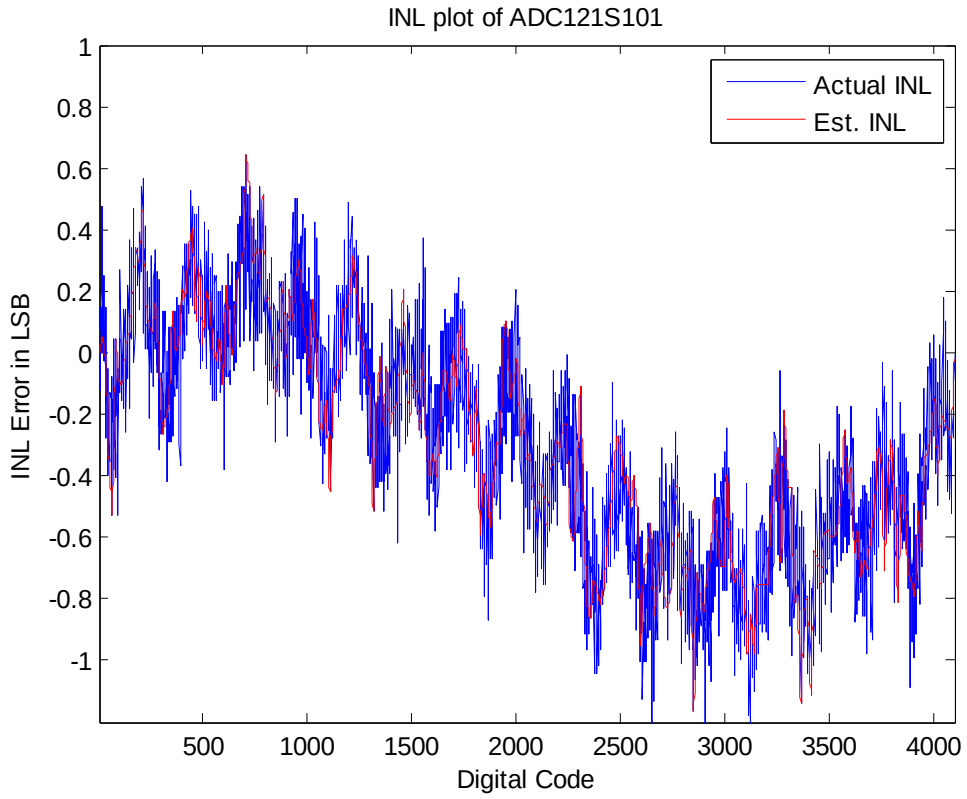

Figure 101. INL Measurements using Histogram Test and Proposed Test in Hardware Experiment.

4.5. SUMMARY

A novel segmentation-based linearity testing technique for the high-resolution A/D converters with low resolutions D/A converters was presented in Chapter 4. The proposed test methodology is based on the least-squared fitting approach with the scaling and segmentation techniques. The proposed linearity test methodology precisely estimated the linearity specifications of the high-resolution A/D converters even when the non-ideal D/A converters were used, which reduces the cost of test equipment and relaxes the tight requirement for the test input source. Further, the proposed methodology significantly reduces the test data volume in comparison to the standard histogram test methodology. Both low-cost test equipment and the reduced test measurement can lead to the cost reduction of the testing and eventually the total reduction of the final products. The proposed methodology was validated in simulation and hardware experiment. The degree of the polynomial function, an offset voltage value, and the number of segmentations must be carefully determined. Future work includes development of intelligent techniques to determine such parameters.

CHAPTER Ⅴ

OPTIMAL LINEARITY TESTING OF SIGMA-DELTA INCREMENTAL A/D CONVERTERS USING RESTRICTED CODE MEASUREMENTS

Chapter 5 presents a methodology for analyzing the goodness of a particular choice of test code points for the linearity testing of high-precision A/D converters. As discussed in previous Chapter 4, the linearity testing of the high-precision A/D converters, beyond 20-bit resolution, is extremely expensive and exhausting due to (1) the large number of digital codes that need to be tested and (2) the associated low-data rates making the traditional histogram-based testing infeasible. The Chapter 4 proposes a low-cost linearity testing methodology for the high-precision A/D converters using low-resolution test input signals. In addition to the use of low-resolution and low-cost test equipment, this test scheme reduces the test measurement as compared to the conventional test method. However, the semiconductor industry sometimes desires much faster production test solutions than the proposed approach described in the Chapter 4 can achieve by reducing the measurement further even if such solutions may require expensive automated test equipments (ATEs). The industry seeks to find cheaper test approaches than the available test solutions. If much faster test approach with more expensive ATEs than the current test solutions can compensate for the use of expensive ATEs and reduces the overall test cost more than the current solutions, then this faster test approach using the expensive ATEs is ideal and preferable for the industry to pursue.

Sigma-delta-based incremental A/D converters are extremely high-resolution converters, commonly 24-bit or higher, with extremely lower-sampling rates than the other types of A/D converters. The incremental A/D converters have speeds of a few hundred samples per a second (PSP) in general and are used in sensing, instrumentation, and measurement applications due to high-precision capability. Because of such significantly low-sampling rates, test solutions with as little measurement as possible are needed even at the cost of expensive equipment to speed the total test time up. As a result, the industry often performs the linearity test for such high-precision and low-speed data converters with significantly reduced number of code measurements during the production test using expensive equipment if such test methodology can save the overall test cost more than the cost of other solutions. Given a specified allowed number of code measurements, the problem is to determine the requisite code points that achieve the highest failure coverage. Therefore, Chapter 5 presents the proposed methodology to determine the minimum optimized test code points for the maximum fault coverage.

In the proposed approach in Chapter 5, a least-squares-based polynomial fitting approach using measurements made at selected test code points is used to characterize the transfer function of the A/D converter for the integral nonlinearity (INL). The proposed test solution that can be adopted by the industry is developed as a production test solution. The methodology proposed in Chapter 5 determines the best test codes to measure that estimates the nonlinearity of the A/D converters as accurately as possible given a maximum number of allowed code measurements. In addition, the characteristics of the devices that may escape from the proposed approach, called test escapes, are revealed for the specified

test via an optimization-based search technique. The goals and objectives of the proposed research work are outlined as follows:

1. The proposed methodology develops a fast INL test solution for the high-precision and low-speed A/D converters such as the incremental A/D converters that can be adopted by the industry as a production test solution.
2. The proposed methodology allows an accurate INL estimation for the high-precision A/D converters with extremely small number of code measurements with minimal loss of failure coverage by defining the minimum necessary test code points.
3. An optimized-based search technique is developed to catch the test escapes and reveal the characteristics of such devices.

In the following, prior research works involving the linearity test of the A/D converters with the reduced number of measurement are briefly introduced in Chapter 5.1, and the problem associated with testing of the incremental A/D converters is discussed in Chapter 5.2. Then, Chapter 5.3 presents the detail of the proposed methodology, and the simulation results are provided in Chapter 5.4 to validate the proposed methodology.

5.1. PREVIOUS WORK

Various research approaches from the past that are capable of the linearity test for A/D converters with less measurement than the mandatory measurement in the conventional histogram test method are introduced in Chapter 5.1.

The traditional histogram test requires collecting the minimum average number of 30 samples per a code. This implies that the minimum required measurement is 2^Nx30, where N is the resolution of the A/D converter. For testing 24-bit resolution A/D converters, the minimum number of output sample measurement must be over 503 million codes (503,316,480). This number may be significantly increased for more accurate test result than the histogram test with the measurement of 30 samples per a code. This minimum required measurement can be significantly reduced using techniques based on the linear modeling proposed in [23]-[28]. The test methodologies based on the linear modeling in [23]-[28] build a linear model in terms of code transition points and errors, and then methods measure only a defined subset of transition levels that is much less measurements than the histogram test requires. Accordingly, the test time can be reduced compared to the histogram test. Such linear modeling test requires only a few multiple times of the total digital codes of A/D converter. This measurement volume can be further reduced using a stimulus error identification and removal (SEIR) proposed in [17]. The SEIR methodology in [17] requires the sample measurement that is equal to the number of digital codes in A/D converters under test, which is 2^N, where N is the resolution of the A/D converters. However, this total measurement is still large for the 24-bit incremental A/D converters. Authors in [64] propose a methodology that reduces approximately 75% of the total test time from the conventional test by measuring only selective code points. The proposed methodology in [64] makes measurements on a subset of the total codes that are affected by manufacturing process variations in successive approximation register A/D converters (SAR) using a property that the nonlinearities of the SAR A/D converter are closely

correlated to the manufacturing process variations. The proposed test methodology in Chapter 4 reduces the test measurement significantly from the minimum required measurement in the histogram test. With the use of two 10-bit D/A converters as test input generators, the total number of measurement can be $2x2^{10}xR$, where R is the number of repeated test to compensate for the noise performance of the two D/A converters. Even if the test is repeated 100 times to average the measurement, the total test measurement is only 204,800. However, the limitation of the methodology is to find the optimal values for the number of windows, degree of the polynomial function, and an offset voltage. Furthermore, the total number of measurement may have to be increased to enhance the accuracy of the specifications estimation.

In this Chapter 5, the test methodology that requires much less measurement than the conventional histogram test and above test solutions is proposed. The proposed methodology can be used as a suitable production test solution for extremely high-precision A/D converters with low-sampling rates. In next, the overview of the high-resolution and low-speed incremental A/D converters and the problem associated with testing the incremental converters are discussed.

5.2. PROBLEM DEFINITION

In Chapter 5.2, a motivation for the proposed methodology is presented with the brief overview of the incremental A/D converters. First, the overview of the incremental A/D

converter is introduced, and then the testing issues for the high-precision incremental A/D converters are discussed.

5.2.1 Overview of Incremental A/D Converters

The sigma-delta A/D converters can achieve high-resolutions with high-SNRs as a result of their oversampling and noise shaping properties that pushes noise power to out-of-band, which is removed by the digital filter and digital decimator. However, the incremental A/D converters are more suitable than the sigma-delta A/D converters in instrumentation and measurement applications due to excellent offset and gain error tolerance [65]. Both the sigma-delta A/D converters and the incremental converters use the sigma-delta modulation architecture. However, the operation of the incremental A/D converters is slightly different from the operation of the sigma-delta A/D converters as follows [65]:

1. The switched-capacitor integrator and the digital counter at the output are reset at every new conversion.
2. A fixed number of integration steps are performed, and the input is held for each conversion.
3. The decimation filter is simpler than sigma-delta A/D converters, which is commonly one-order higher Sinc filter than the order of the sigma-delta modulation used in the converters.

As a result, the incremental A/D converters require more number of cycles to settle than the conventional sigma-delta A/D converters, so the incremental converters have extremely

low-speed operation. The speed of the common incremental A/D converters is generally 15 PSP to a few hundred PSP at the most. However, the incremental A/D converters take the most advantages of the sigma-delta A/D converters and capable of the offset-free and accurate conversion, which make the incremental A/D converters perfect candidates for extremely accurate measurement applications at the penalty of slow-operation.

5.2.2 Problem Definition

The incremental A/D converter is based on the sigma-delta modulation architecture and has many aspects in common with the sigma-delta A/D converters as discussed above. Both the incremental converters and sigma-delta A/D converters can achieve much higher resolution than the other A/D converter architectures. The number of digital codes is associated with the resolution of the A/D converter: the number of the digital code increases as the resolution of the A/D converter increases. The most challenging problem for testing the high-resolution incremental A/D converters is the large number of digital codes that must be tested. Further, the high-resolution incremental A/D converters generally have a low-sampling rate, which in turn implies a long test time. As described in Section 5.2.1, the incremental A/D converters are far slower than all other architectures of A/D converters (maximum output data rate of less than 1k samples per second). In addition, voltage drifts in the tester must be taken into account. Although advanced automated test equipment (ATE) may supply a stationary reference voltage over small periods of time, small drifts over a long test time can substantially affect the overall test quality since the

high-resolution incremental A/D converters are extremely sensitive to a small voltage change. As a result, the histogram-based test method is not feasible for such converters, and thus a fast test approach that can reduce the volume of test data collection is highly necessary. Section 5.1 introduces the prior research works that aim for fast linearity tests of the A/D converters. The techniques from the past are novel and reduce the output measurement compared to the traditional histogram test. In this proposed methodology, the output measurement is further reduced, and the minimum test code points are determined.

5.3. PROPOSED METHODOLOGY

Detail of the proposed methodology is explained in Section 5.3. The behavioral model of the incremental A/D converter that is used in development of the proposed methodology is provided in Section 5.3.1. In Section 5.3.2, a possible histogram-based test approach with the reduced number of measurement is briefly discussed. Then, the technique for test code selection is presented in Section 5.3.3, and an optimized search algorithm for revealing the test escapes is introduced in Section 5.3.4.

5.3.1 Behavioral Model of Incremental A/D Converters

The incremental A/D converter is based on the sigma-delta architecture as described in Section 5.2.1. To validate the approach of the proposed methodology, the behavioral model of 24-bit 3rd-order cascaded-integrator feed-forward (CIFF) sigma-delta incremental

converter is modeled in Matlab and Simulink. Figure 102 shows the model of the incremental A/D converter incorporating key module level nonlinearities. The detail description of the nonlinearities modeling is discussed in Chapter 2, so the modeling description is skipped in Section 5.3.1. The model in Figure 102 differs from the 2^{nd}-order sigma-delta A/D converters as shown in Figure 20 only in terms of the architecture and the operations described in Section 5.2.1. The main nonlinearities modeled in Figure 102 are summarized as follows:

1. Clock jitter at the input sampler
2. Thermal noise (kT/C noise) in switched-capacitor circuit
3. Operational amplifier DC gain
4. Operational amplifier slew rate
5. Operational amplifier gain bandwidth
6. Operational amplifier input referred noise
7. Operational amplifier saturation voltage level
8. Operational amplifier total harmonic distortion
9. Operational amplifier offset
10. Operational amplifier PSRR
11. Operational amplifier CMRR

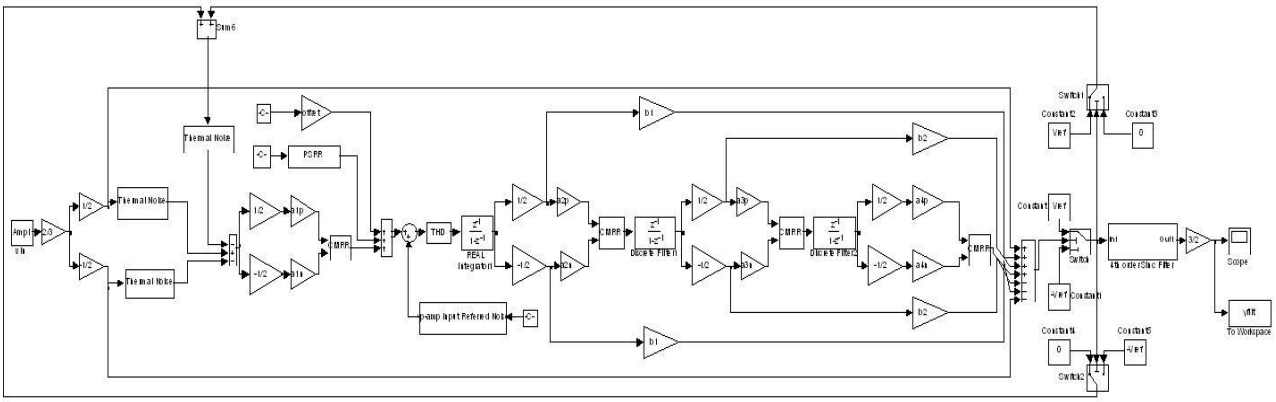

Figure 102. Behavioral model of 24-bit 3rd order differential CIFF incremental A/D converter

5.3.2 Test with Reduced Number of Digital Codes

Full histogram-based test is not suitable for testing extremely high-resolution A/D converters as stated in Section 5.1. However, the histogram test method may become practical when the resolution of A/D converters under test is forced to be less (reduced code measurements) than the full-code measurement. Figure 103 illustrates the basic concept of such approach using a 4-bit resolution A/D converter test as an example. In this Figure 103, the 4-bit resolution of the converter is reduced to 2-bit resolution by treating a digital code 0 to a code 3 of the 4-bit A/D converter as a code 0 and treating a code 4 to a code 7 of the 4-bit A/D converter as code 1 and so on. As a result, a 2-bit equivalent histogram can be constructed for the 4-bit A/D converter histogram. For the same test time, one can achieve 115 samples per a code for the 2-bit equivalent A/D converter or 30 samples per a code for the original 4-bit A/D converter. In contrast, for the same number of 100 hits per a code, testing the 4-bit ADC requires the total of 1600 samples, while testing the 2-bit equivalent

A/D converter requires only 400 samples. However, a relatively *good approximation of INL* can be extracted with significantly reduced test data volume in the latter case. This approach suits well for the oversampling type of A/D converters such as the sigma-delta A/D converter and the incremental converter because they do not have a missing code issue.

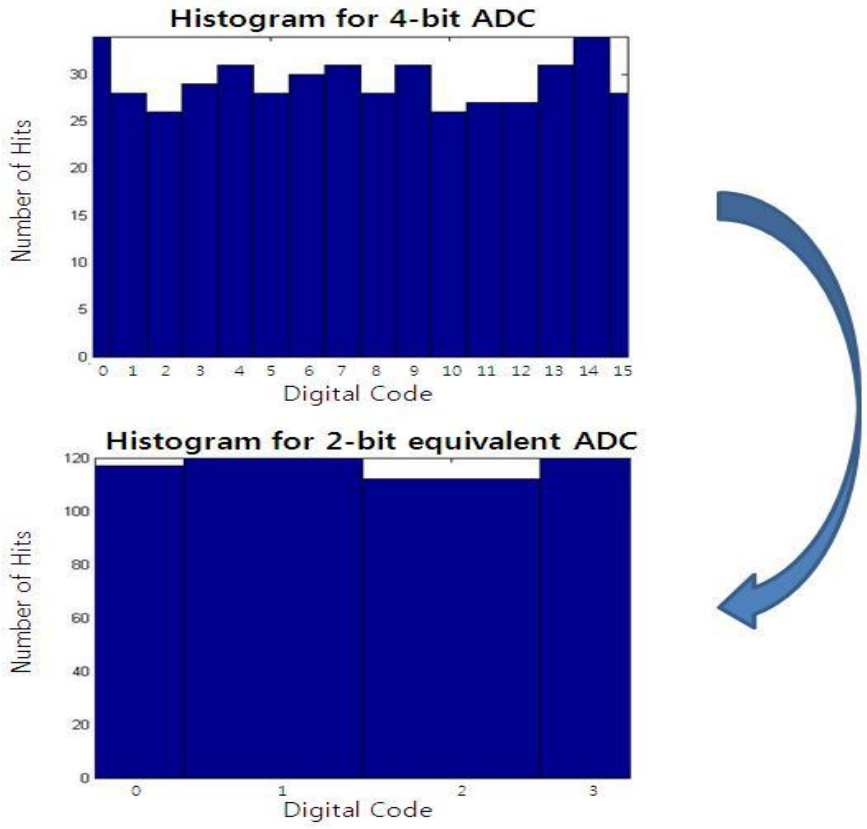

Figure 103. Resolution reduction

Figure 104 – Figure 107 depict INL plots of the identical 24-bit resolution A/D converter using the approach of the reduced resolution histogram. In all cases, an average number of 100 samples per a code is collected. These results indicate that the INL errors

are well approximated with significantly fewer samples although DNL errors are not explored. However, such approach may not be better than the prior proposed works discussed in Section 5.1 and does not investigate up to which resolution can be reduced to. Some of the past proposed researches introduced in Section 5.1 might work better with less measurement than the reduced-resolution histogram approach. Next Section 5.3.3 explores the proposed methodology using the concept of the reduced-resolution histogram approach.

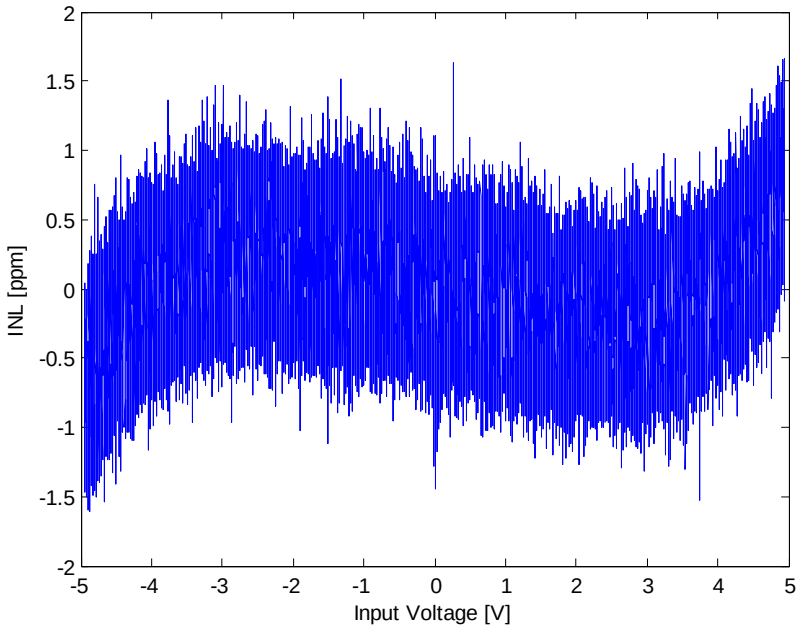

Figure 104. INL plot of 24-bit A/D converter (≈ 1.6e9 samples)

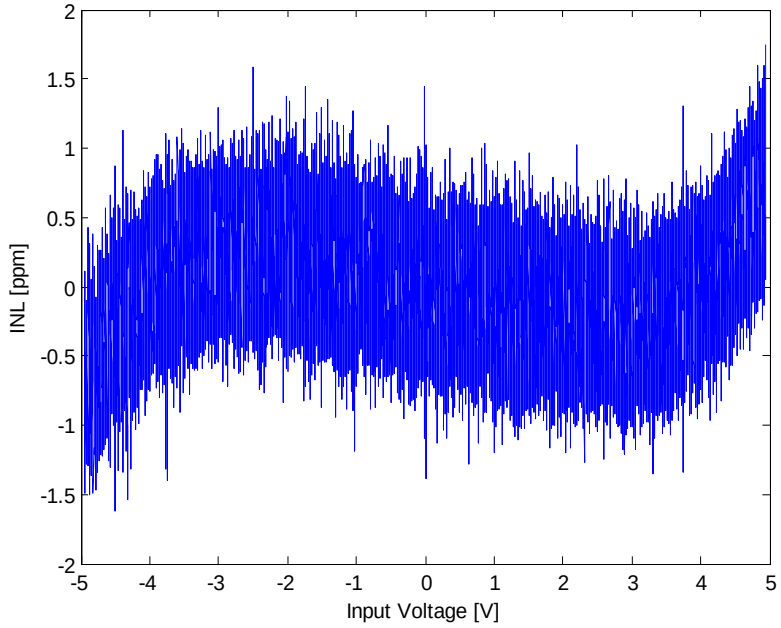

Figure 105. Equivalent INL plot using 16-bit resolution (≈ 6.6e6 samples)

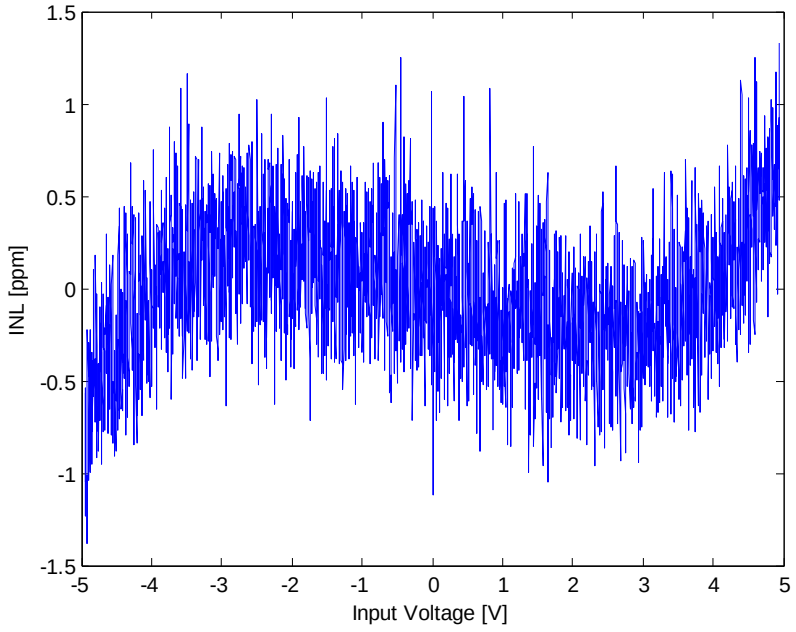

Figure 106. Equivalent INL plot using 12-bit resolution (≈ 410e3 samples)

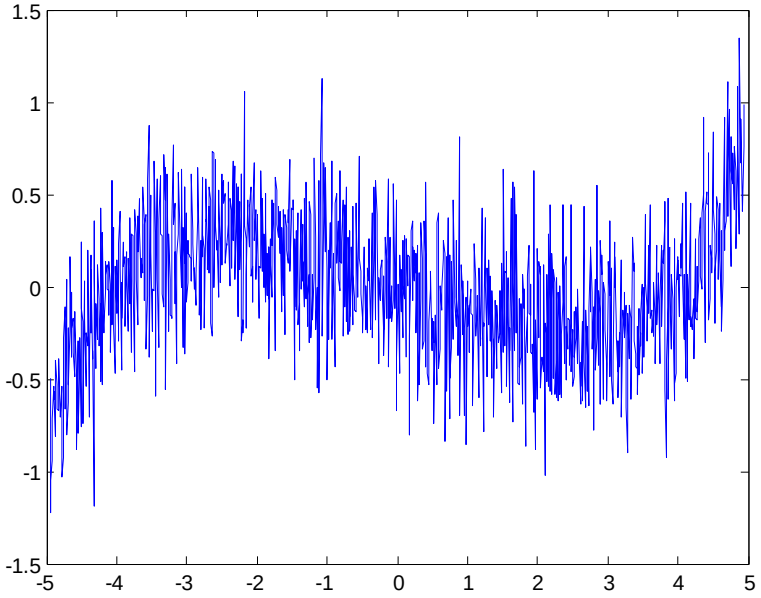

Figure 107. Equivalent INL plot using 10-bit resolution (≈ 102e3 samples)

5.3.3 Best Curve Fitting Approach with a Few Code Measurements

High-resolution oversampling type of A/D converters is inherently linear and missing-code free. Such A/D converters do not have sharp transitions in INL plots unlike other types of A/D converters that might have such sharp transitions in INL plots as a result of mismatch of internal components such as capacitors and/or resistors. Therefore, a best curve fitting method can well characterize the transfer function of the high-resolution oversampling type A/D converters, while the best curve fitting method may fail for other A/D converters such as pipeline A/D converters. Since the high-resolution incremental A/D converters and sigma-delta A/D converters have smooth INL curves and do not have the missing-code problem, the polynomial-based curve-fitting technique is a good candidate.

The INL plot shown in Figure 104 obtained from the original histogram test has a smooth sine-wave shape in overall, and the INL errors corresponding to the input voltage of -5V to 0 is symmetric to the other side of INL errors corresponding to the input voltage of 0V to 5V since the 24-bit incremental converters in Figure 102 has a differential input path. Therefore, a few code measurements distributed across the full-scale of the A/D converters can be used to track such A/D converter transfer function using the best-curve-fitting technique. Note that the estimation from the best-curve-fitting technique can track the actual INL plot, but it does not explore the DNL information because the estimated transfer function is a smooth version of the actual transfer function.

Figure 108 presents the INL plot using the best-curve-fitting technique to characterize the identical 24-bit incremental converter shown in Figure 102. Figure 108 compares the INL plot in Figure 106 with the INL estimated using the polynomial fitting *across only four precise input signal values* (-5V, -2.5V, 2.5V, 5V). One major limitation of the technique as compared to the proposed methodology in Chapter 4 is to use high-precision test stimulus that increases the overall test cost. However, such four point measurements are significantly smaller than the number of measurements used in the proposed methodology in Chapter 4. As a result, the overall test cost can be further reduced by testing A/D converters at much faster test time than the proposed method in Chapter 4. In this estimation shown in Figure 108, 3^{rd}-order polynomial function can be used, and 100 measurements for each point were taken and averaged to suppress the noise effect. In this case, the INL was not estimated from the histogram-based technique but from the polynomial fitting of four points corresponding to the four precision DC input values. The

results indicate that the surprisingly small amount of test data can be used to accurately predict INL of the 24bit A/D converter. In comparison to the proposed method in Chapter 4 that requires the output samples of 204,800, this four-point-measurement test requires only 400 output samples at the penalty of using high-precision and expensive test equipment. The polynomial-fitting-based test is a popular method to characterize such transfer function of the system or A/D converters [41], [62], [66].

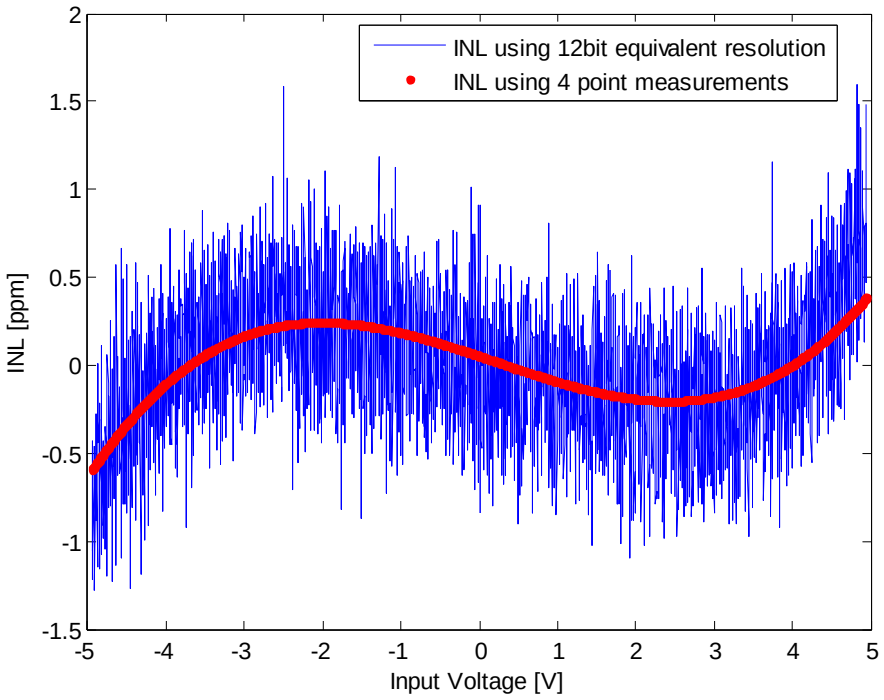

Figure 108. Equivalent INL using 12-bit resolution (blue) and INL estimation using four-point measurements (red).

However, a key question is whether these four-code measurements with the polynomial-curve fitting are sufficient to predict *all* ADC anomalies induced by small and large process

variations and parasitics. To investigate the effects of the process variations, the values of the nonlinearity in Figure 102 are varied to find devices whose INL estimations are failed using the polynomial-curve fitting with four-point measurements.

Figure 109 shows two devices under a test setup identical to that of Figure 108. It is seen that the proposed polynomial-fitting approach with the four-point measurements fails to estimate the actual INLs of these devices. Figure 110 depicts the INL estimations of the identical two devices in Figure 109. Only difference between Figure 109 and Figure 110 is that the INL errors in Figure 110 are estimated with the increased number of measurements and higher-order polynomial-fitting method than the INL errors estimated in Figure 109. The INL in Figure 110 is estimated using the proposed methodology after finding the optimal best code points, which will be provided in Section 5.3.6. The estimation in Figure 110 was obtained by measuring six-point measurements with 5^{th}-order polynomials, while only four-measurements and 3^{rd}-order polynomial fitting are used to estimate the INL in Figure 109. This implies that the number of test measurement points and the choice of test codes are critical for the accurate INL prediction and the success of the proposed approach. In the following section, a viable test code selection strategy is presented.

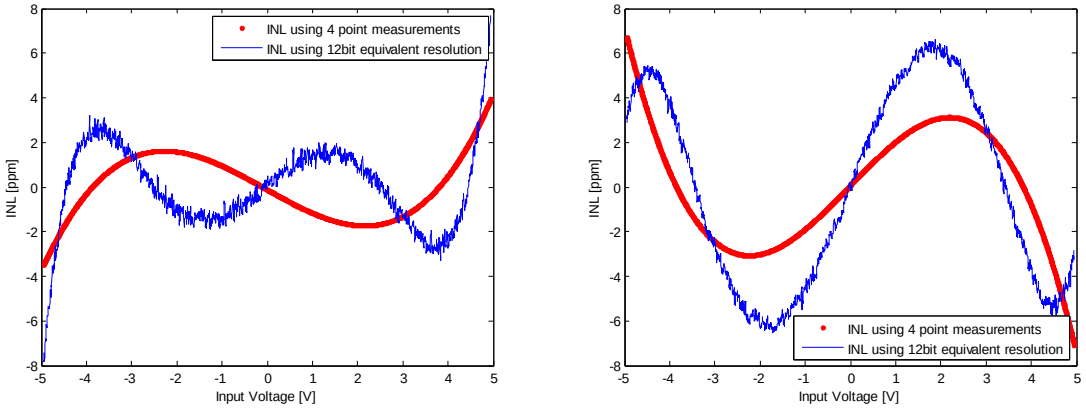

Figure 109. INLs comparison using 12-bit equivalent histogram (blue) and using four-point measurements.

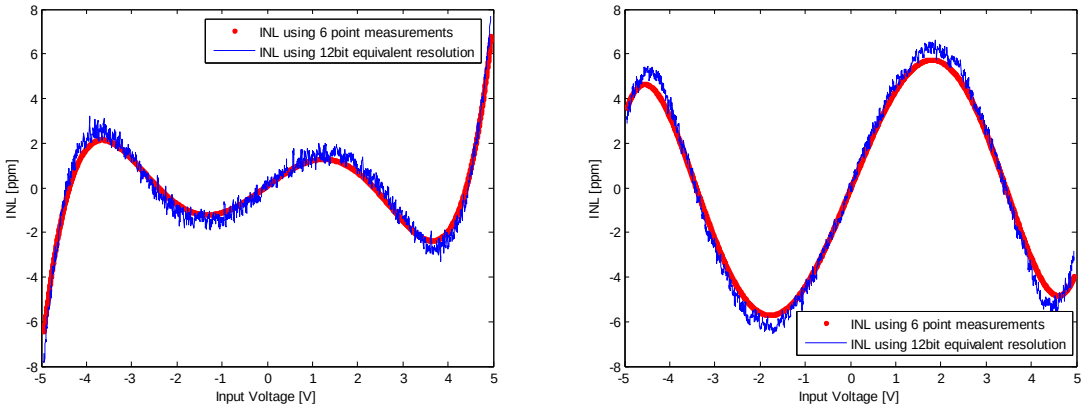

Figure 110. INLs comparison using 12-bit equivalent histogram (blue) and using six-point measurements of the proposed methodology.

5.3.4 Test Code Selection

Section 5.3.4 describes a proposed methodology to determine the test-code points that must be measured to estimate the actual INLs of the incremental A/D converters precisely. The methodology is developed to achieve the maximum fault coverage.

To find the optimal set of test-measurement points for the maximum fault coverage, the use of principle component analysis (PCA) is developed in this proposed methodology. The principle component analysis is a well-known statistical technique that is widely used in data analysis and compression. The PCA reduces the dimensionality of data, while retaining as much information as possible of the variations present in the original data set through an orthogonal transformation. All the possible digital codes of the incremental 24-bit A/D converter are considered as variables, and the PCA analysis converts these into a subset of new variables (principal components or test code points), in such a way that the transfer function of the A/D converter can be reconstructed from the principal components, which are significantly fewer in number than the full set of digital codes of the 24-bit A/D converter. The principal components can be easily calculated using the PCA toolset available in the MATLAB statistics toolbox.

The proposed approach begins with the use of the first three principal components, which are subsequently used to fit a 2^{nd}-order polynomial function for the A/D converter transfer function. The larger the number of principal components that are considered, the higher the total measurements samples that are needed, and the better the INL estimation can be achieved for the A/D converter under test. The goal is to keep the number of

principal components to a minimum number to reduce the total test time and measurement. Further, the use of many principal components does not always result in the best INL estimation since (1) the first few principal components are generally dominant and give a good approximation to the overall INL statistics and (2) the use of high-order polynomial functions can result in the over-fitting problem. Note that the maximum possible degree of the polynomial function, which is the number of principal components – 1, is used all the time, but the highest degree is limited to a 5^{th}-order polynomial to avoid the over-fitting problem that produces even worse INL estimations than low-order polynomial function.

A case in which some or all of the selected principal components, as known as test code points, are located in certain regions of the code space only must be considered, which is not desirable. This undesirable code selection ends up with unavoidable test-fail because the full-scale transfer function must be reconstructed from the test data. For the test code points to be distributed across full-scale, it is necessary to include "anchor points" into the polynomial calculation. These anchor points consist of predetermined input-output values corresponding to non-significant principal components that are used during polynomial fitting but are not measured for each device that is tested.

5.3.5 Search Algorithm for Characterization of Test Escapes

The proposed technique described above defines the optimal test-code selection and achieves the test-time reduction as a result of significantly small number of test

measurements. However, this proposed approach cannot guarantee 100% fault coverage as long as undetectable faulty devices exist. The undetectable faulty devices are defined as the devices that escape from the proposed test approach but whose actual INLs are in fact bad as a result of inaccurate estimations. In this Section 5.3.5, an optimization-based search algorithm is introduced for finding such devices (A/D converters), and a set of the A/D converter nonlinearity characteristics (device vulnerability) that make the faulty DUTs pass the proposed test will be identified.

An augmented lagrange optimization technique is used to find undetectable bad devices as a search algorithm in this thesis. This augmented lagrange approach is useful in this study since the method converts a constrained problem into an unconstrained function. Similar to other constrained optimization problems, the augmented lagrange technique minimizes the objective function subject to constraints. The optimization problem is formed as follows:

Objective function: min{f(x)} Equation 26

Subject function (constrains): G(x) ≤ 0 Equation 27

The augmented-lagrange-based optimization technique minimizes the objective function, while satisfying the subjective function of $G(x)=[g_1(x), g_2(x), \bullet\bullet\bullet, g_n(x)]$. The goal of the proposed technique is to search undetectable faulty devices that escape the proposed INL test (test pass / specification fail). The INL errors obtained from the full-code measurements and obtained from the proposed method are defined as $Full\_Test_k$ and

Reduced_Test$_k$ for a specific device ‘k’. When the maximum allowable INL error is defined as *INL_Limit*, then above objective and constrained functions are constructed as follows:

f(x) = *Max{Reduced_Test*$_k$*} - INL_Limit* $\leq$ **0 Equation 28

G(x) = *INL_Limit - Max{Full_Test*$_k$*}* $\leq$ **0** Equation 29

If the problem is concerned with various specifications, G(x) can be a set of G(x)=[g_1(x), g_2(x), •••, g_n(x)], where n is the number of specifications in consideration. However, since this work is associated with only INL in this thesis, the problem is solved with only one constraint. The augmented-lagrange function can be formulated in various ways, and the function presented in [67] is adapted, which is

$$L(x,\lambda,\gamma) = f(x) + \sum_{i=1}^{N}\left[\max\left(\frac{1}{2}\lambda_i + \gamma \cdot g_i(x), 0\right)\right]^2 \quad \text{Equation 30}$$

, where λ_i is Lagrangian multipliers, γ is penalty parameter, and x is a combination of parameters (nonlinearity). A flow of the algorithm is presented in Figure 111.

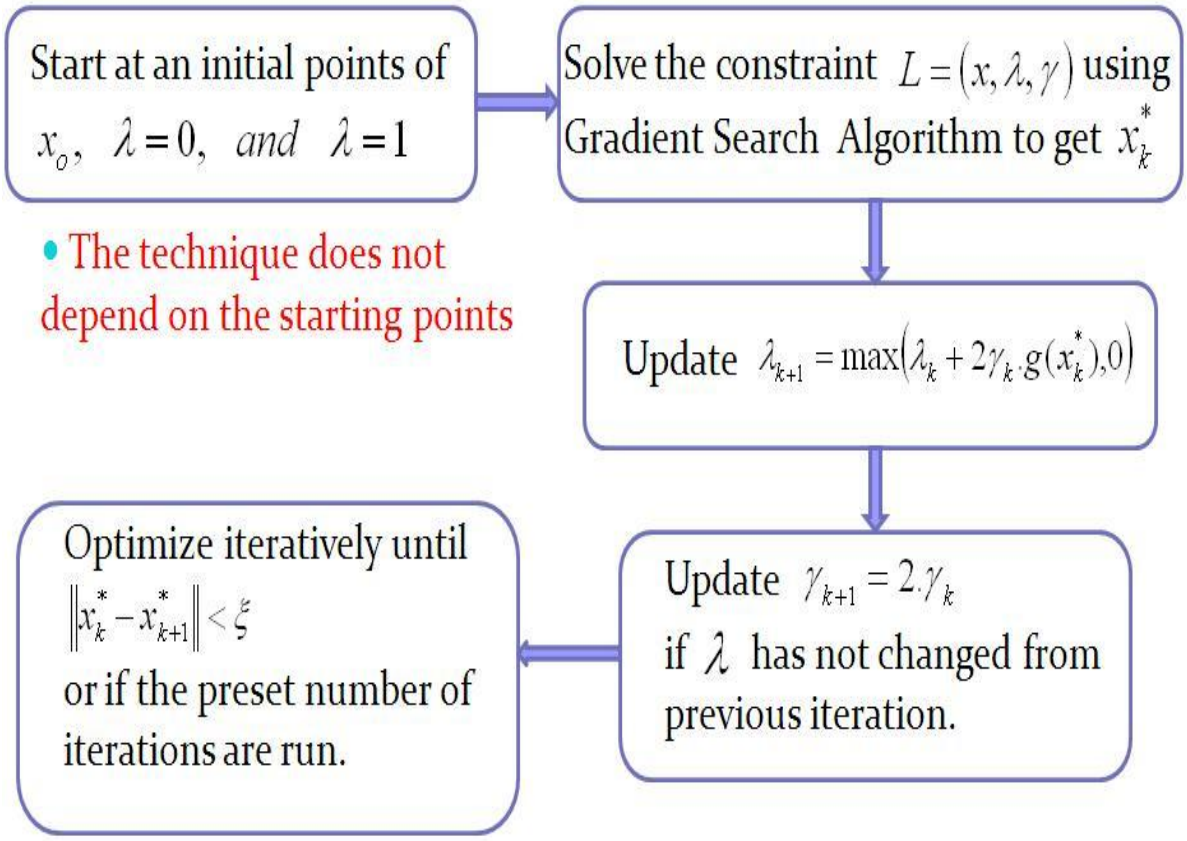

Figure 111. Augmented Lagrange search algorithm flow.

5.4. SIMULATION RESULTS FOR VALIDATION

Section 5.4 presents simulation results to validate the proposed test methodology. The Chapter 5 introduces (1) an INL test methodology for the high-precision incremental converters and (2) an optimization-based search algorithm to define the test escapes from the proposed INL test. In following, the simulation results of both the INL test method and the search algorithm will be presented.

5.4.1 Simulation Results Validation for Proposed INL Test

To study the effects of process variations, a population of 500 devices was implemented using the behavioral model as shown in Figure 102 with the process variations generated from Monte Carlo simulation, each instance with a unique combination of parameter (nonlinearity) values. Table 11 presents the first 10 principal components, also as known as test code points, found from the principal component analysis. The digital codes for the 24-bit A/D converter model range from -8388608 to 8388608, and the input signal range is from -5V to +5V. The full-scale range was divided into 10 sub-regions with at least one code selected from each sub-region. Note that the analog DC values that correspond to such code points found from PCA are candidates for test stimuli.

Table 11. Principal Components

	Test code points	Input signal value
1st principal component	-8297945	-4.94V
2nd principal component	-7205814	-4.295V
3rd principal component	7071597	4.215V
4th principal component	-2910847	-1.735V
5th principal component	2634023	1.57V
6th principal component	5701737	3.3985V
7th principal component	2088763	1.245V
8th principal component	-5695865	-3.395
9th principal component	-1066167	-0.98
10th principal component	1778385	1.06V

Table 12 summarizes the results using different number of principal components. First column indicates the number of principal components, and the degree of polynomial function is given in the second column. The third column presents the number of the devices, in which polynomial function with corresponding principal components fails to estimate the actual INLs. From the Table 11, 5th-order polynomial function with the first 6 principal components give the best INL predictions. Higher degree polynomial functions with 7 or more principal components resulted in over-fitting.

Table 12. Performances of Principal Components

Number of principal components	Polynomial degree	Fault estimation out of 500 devices
3	2	76
4	3	21
5	4	8
6	5	1
7	5	1

5.4.2 Simulation Results Validation for Search Algorithm

In Section 5.4.2, the optimization-based search algorithm using the augmented lagrange technique is validated in the software simulation. For simplicity, an example of the algorithm is experimented using 2500 devices with variations of only two nonlinearities (slew rate and gain bandwidth of operational amplifier). Devices with two nonlinearities allow generating 3-dimentional surface plot and track the search path of the search algorithm. Devices with the maximum INL error of 10 ppm or higher are defined as faulty devices and as good devices with maximum INL error of less than 10 ppm. The 3-D surface plot is presented in Figure 112. The device at the destination in Figure 112 is the escaped device from the proposed INL test approach. Its maximum INL error was estimated as 9.185ppm, but its actual maximum INL error was 12.82ppm. One iteration of the algorithm finds one undetectable faulty device, and the algorithm iterates until no more undetectable faulty device exists.

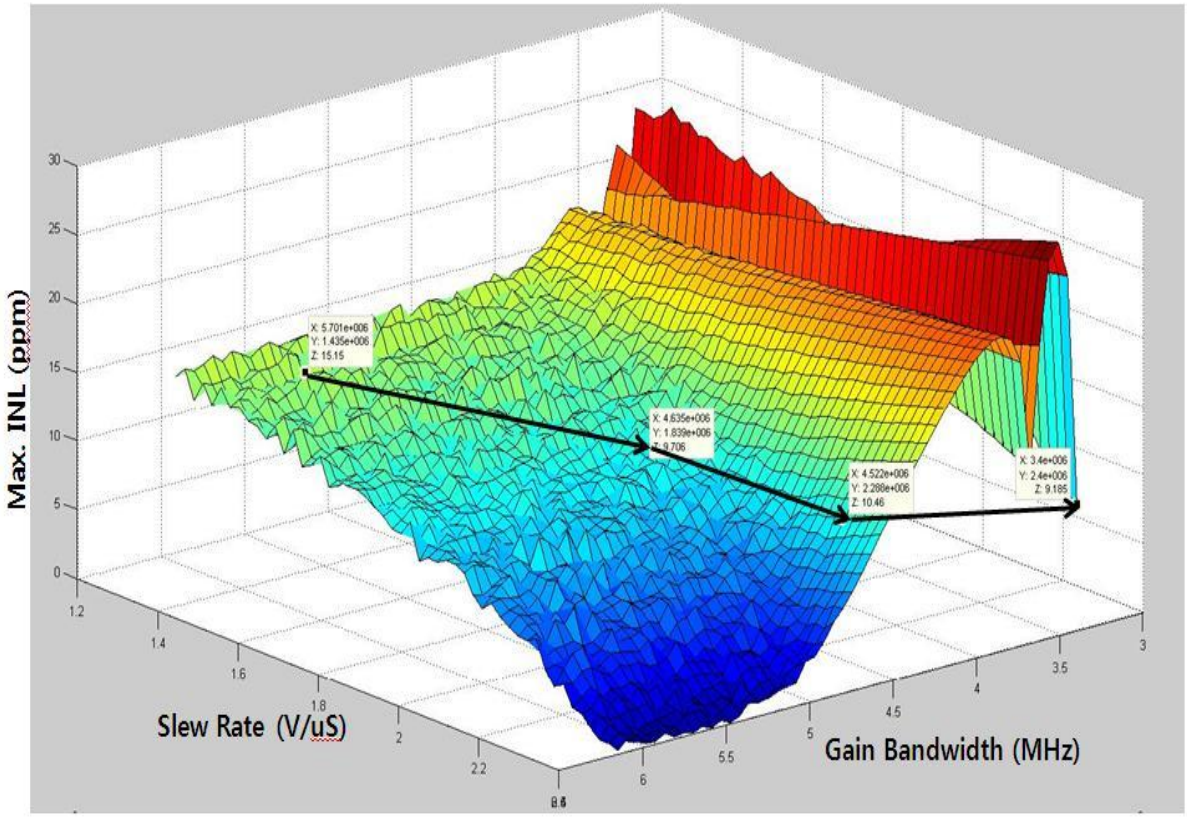

Figure 112. Example of augmented lagrange search result.

The described search algorithm was applied to the identical set of 500 devices used in the previous Section 5.4.1. One faulty device previously passes the proposed test when using the six test-code points with 5^{th}-order polynomial function, and this undetectable faulty device was found using the search algorithm. Figure 113 shows the undetectable faulty device found among 500 instances. The 24-bit A/D converters are consisted of 11 nonlinearities as described in Section 5.3.1, but the resulted plots are presented with only four nonlinearities in Figure 113 to avoid redundant plots. The result reveals the set of nonlinearities for the undetectable faulty device that allow the device to escape from the proposed test approach.

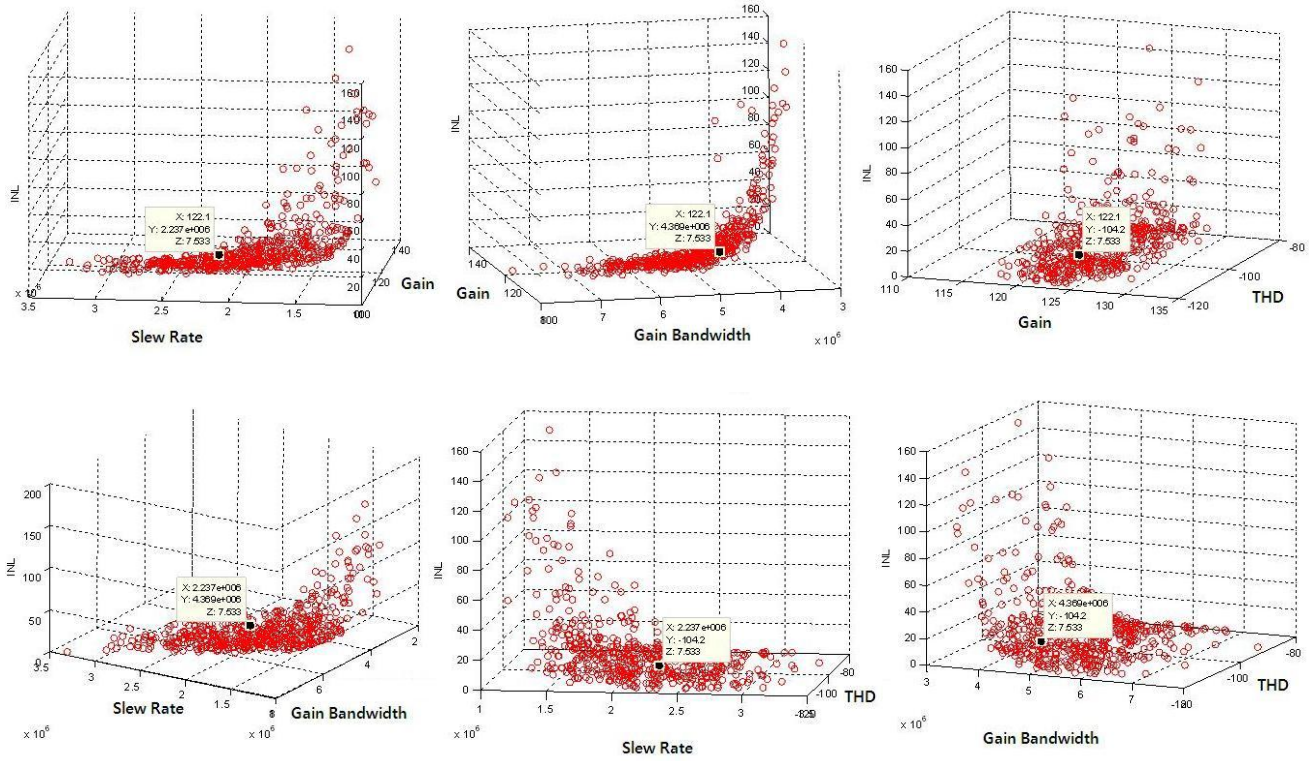

Figure 113. Search for undetectable faulty device.

5.5. SUMMARY

The proposed methodology presented in Chapter 5 significantly reduces the volume of test samples, which eventually reduces the cost of testing and the final cost of the electronic products, as compared to the conventional histogram test method and the proposed methodology in Chapter 4. The proposed methodology is based on a least-squares-based polynomial fitting using measurements made at the optimized code points, and the requisite test code points for the highest fault coverage are determined by principal component

analysis. In addition, an optimization-based search algorithm is developed to detect the devices that escape from the applied proposed test method and to reveal the characteristics of such devices. This proposed test methodology is extremely fast since only a few optimized test points are measured, and hence the methodology is a good candidate for the production test solution. The use of the high-resolution expensive input signal is one limitation, and the DNL error cannot be extracted from the proposed methodology.

CHAPTER Ⅵ

CONCLUSION

In this dissertation, a low-cost test framework for high-resolution A/D converters is proposed. For testing high-precision A/D converters, the input stimulus must have better resolution and higher purity than the devices under test (DUTs), and as the resolutions of the A/D converters increase, the test time is accordingly increased. As a result, testing the high-resolution A/D converters is extremely expensive and exhausting. The objective of the proposed research work in this thesis is to develop efficient test procedures for testing of the high-resolution A/D converters that can reduce the overall test cost by significantly reducing the test measurement and/or using low-cost equipment.

In Chapter 2, an alternate-based test approach is developed for the dynamic specifications of the high-resolution sigma-delta A/D converters. The technique uses a low-cost test stimulus generated by an optimization-based genetic algorithm. The output data stream of the sigma-delta modulator, whose sensitivity is increased by the optimized input stimulus, is used as a test data before they are removed by the digital filter and digital decimator. A regression-based algorithm, MARS, builds a strong correlation mapping function between the specifications of the DUTs and the measurements of the DUTs. 20 DUTs using a training set of 40 devices are precisely estimated in the hardware experiment.

In Chapter 3, the model-parameter-based methodology for the dynamic specifications of the high-resolution A/D converters is proposed. The proposed methodology is based on a signature-based test approach, and this signature-based test

strategy adopts the test setup in the above alternate-based test method such as the use of the modulator output as a test access point and the test generation using the genetic algorithm. However, this methodology eliminates the use of a supervised learner with a training set of devices required in the alternate-based test. The proposed methodology accurately estimates the specifications of the high-resolution A/D converters. Furthermore, the nonlinearities of the sigma-delta A/D converters are revealed allowing to diagnosis defective devices.

In Chapter 4, a low-cost linearity test methodology is presented for the high-resolution A/D converters. The test strategy uses two low-resolution (low-cost) D/A converters, and two identical sets of test input, which are scaled by an offset voltage, are applied to the A/D converters under test. The transfer function of the high-resolution A/D converters is accurately characterized using a polynomial-fitting method with the developed scaling and segmentation techniques. In the test scheme, the cost of testing is reduced since no expensive high-precision stimulus generator is required, and less measurement than the conventional test can be collected.

In Chapter 5, a fast test strategy is developed based on a best-curve-fitting approach. The proposed methodology provides the best optimal test code points for test measurement, and hence significantly reduced number of measurement at restricted test code points can be made with a penalty of using high-precision signal generator. As a result, the proposed methodology defines the minimum necessary test code points for the maximum fault coverage. Furthermore, an optimization-based search technique that defines the test escapes and reveals the characteristics of such devices is presented.

The proposed methodologies in this thesis ease complex test problems for both the dynamic specifications and static specifications of the high-resolution A/D converters and contribute to the overall test cost reduction. The validations of the proposed methodology provided in this thesis ascertain the effectiveness and the usefulness of the approaches.

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VITA

Sehun Kook was born in Gwangju, Korea in 1976. He received a Bachelor of Science in Electrical Engineering from the University of Arizona, Tucson AZ in May, 2005 and a Master of Science in Electrical and Computer Engineering from Georgia Institute of Technology, Atlanta GA in December, 2007.

In the Summer of 2010, he interned as a test engineer in National Semiconductor, Santa Clara, CA. His research interests include design for test, optimal test stimulus generation, and fault modeling of mixed-signal circuits and systems.